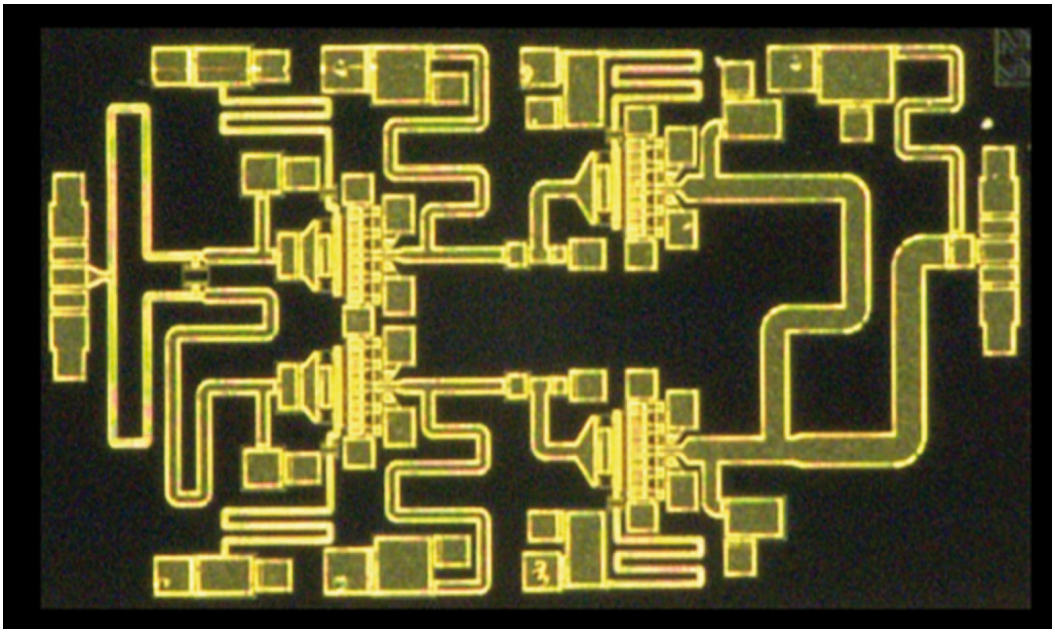
With Cadence AWR Design Environment V15

Intelligent System Design Empowered



Cadence has released the latest version of the AWR Design Environment, Version 15 (V15), the first release since the company acquired AWR Corporation from National Instruments earlier this year.

Cadence Design System
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This latest version, which is available for current customers and evaluators, includes key new features, add-on modules, and enhancements to AWR Microwave Office circuit design software, AWR Visual System Simulator (VSS) system design software, AXIEM 3D planar method of moments (MoM) and Analyst 3D finite element method (FEM) electromagnetic (EM) simulators.

Addresses Product Development Challenges

New capabilities introduced in the new AWR Design Environment V15 address the development of RF/microwave intellectual property (IP), as well as integration at the monolithic microwave integrated circuit (MMIC)/RFIC, package/module, and printed circuit board (PCB) technology levels driven by 5G, automotive, and aerospace and defense applications.

The new AWR Design Environment V15 addresses product development challenges linked to fulfilling the technical demands of 5G communications, which combine fixed, mobile, optical, microwave, and IP transport technologies to deliver ultra-dense, high-capacity, low-latency connectivity. An intelligent network of macro- and small-cell sites, leveraging advanced RF front-end component and antenna technology that is designed for spatial/spectral efficiency and minimal power consumption, is needed to support the high capacity demands of 5G across a vast array of applications and deployment scenarios. As such, the AWR Design Environment V15 expands support for power amplifier (PA) and antenna/array design, PCB, module, and silicon (Si) EM modeling, and RF/microwave IP integration within heterogenous systems.

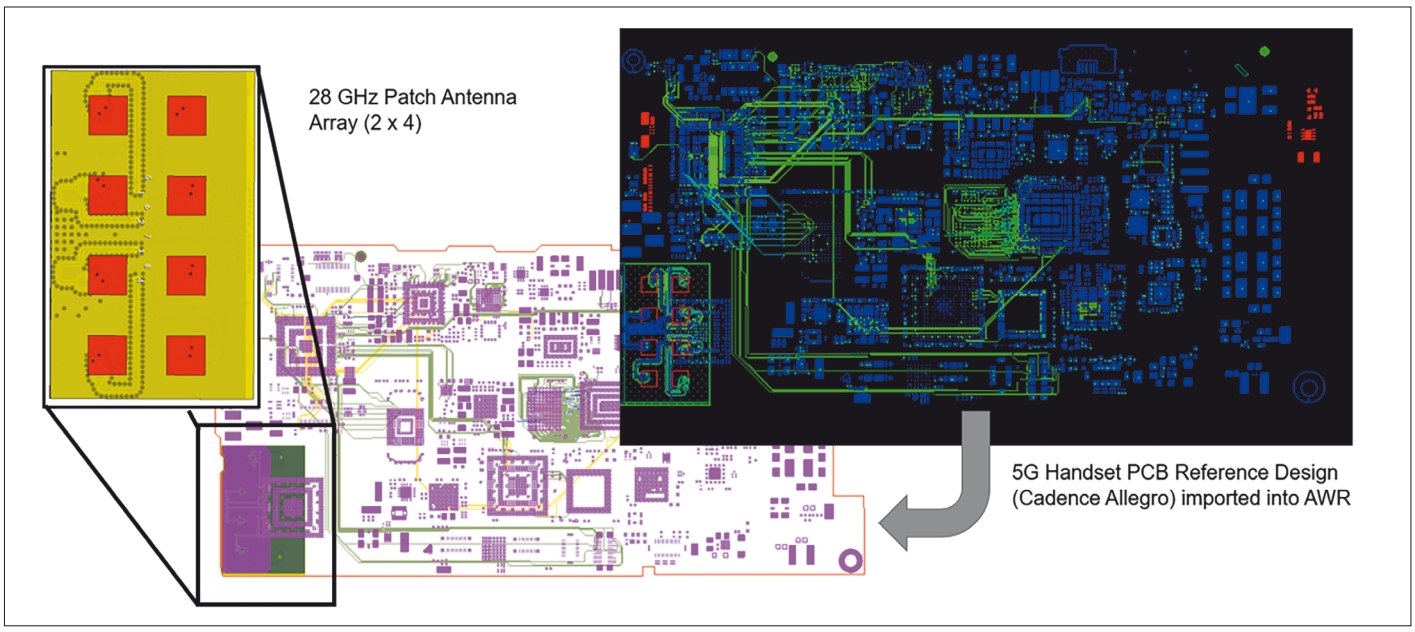
Past is Present – and Future

Technology serving the 5G, automotive, and aerospace and defense markets stems from a long, steady journey of development among platform integrators, semiconductor manufacturers, and companies providing electronic design automation software (EDA) and test and measurement instrumentation (T&M) product development tools. In the late 1980s, the Department of Defense launched the MIMIC program "to develop microwave/millimeter-wave (mmWave) subsystems for use in military weapon system 'front ends' that are affordable, available, and broadly applicable."

The program supported research in materials such as gallium arsenide (GaAs), device design, integration, defect management, manufacturing, and other areas. The overall goal of this program was to provide analog microwave and mmWave sensors, based on GaAs MMIC technology that would improve performance, size, weight, cost, and reliability for U.S. defense systems, specifically targeting computer-aided engineering (CAE) as an area for development. The effort ultimately yielded a new infrastructure for MIMIC technology, with applications proliferating throughout the military and launching the commercial communications market [1].

This MMIC program directed RF simulation software vendors to team up with prime defense contractors and foundries to forge new collaborations in the pursuit of greater platform functionality. Joining this effort was newly formed Cadence (1988), which was tasked with developing simulationable microwave artwork ("smart") libraries, combining an electrical model for MMIC components with a physical layout. Three decades later, defense and communication systems are the result of technologies developed by this alliance between system integrators, semiconductor manufacturers, and tool providers.

Development of the electronics in these systems involves a very complex process, a wide array of tools that transform, analyze, optimize, and verify the design throughout the process, and IP to reuse and reduce



Reference design for 5G handset PCB is imported into the AWRDesign Environment for EM analysis of 8-element (2 x 4) antenna array and feed structure

the scope of design work. For example, systems are increasingly radio enabled, be it 5G, Bluetooth, Wi-Fi, or other standards. The RF front-end components responsible for this wireless connectivity are among the most challenging to design, since every design aspect is interdependent upon each connector, package pin, and PCB trace. A holistic approach to design and analysis of the entire system is required.

Cadence is addressing these changes through the Intelligent System Design strategy, which delivers its world-class computational software capabilities across all aspects of the design of electronic systems. At the core of this strategy is the concept of design excellence, an optimized EDA portfolio of tools inclusive of best-in-class RF/microwave circuit, system and EM analysis, and IP for semiconductor, package, and PCB design, with scalable access in the cloud.

The Wireless Revolution will be Integrated

The latest RF/microwave technologies for 5G infrastructure and mobile devices represent a significant uptick in engineering complexity. Along with this increased complexity, RF electronics will be integrated within an unprecedented number of connected smart devices and systems. To achieve these objectives, highly complex, electronic-centric systems require an equally significant advance in multi-domain analyses, simulation capacity, design automation, and seamless interoperability between RF/microwave EDA and the broader portfolio of mixed-signal IC, PCB, system-in-package (SiP), and system-on-chip (SoC) design tools.

The current "More than Moore" pace of electronic design is made possible through technology integration using densely populated, heterogeneous substrates. These tightly stacked components behave as mechanical systems built with sophisticated electronics transporting RF/high-speed signals through a complex network of interconnects. To function properly, mixed-technology systems require co-design and co-optimization across multiple domains, including RF, analog, and digital simulation, aided by large-scale EM and thermal analysis, and robust design verification and signoff. The AWR Design Environment V15 complements the extensive Cadence software portfolio, providing engineers with the sophisticated tools needed to successfully tackle these design challenges.

Faster EM Analysis for Mixed Technology

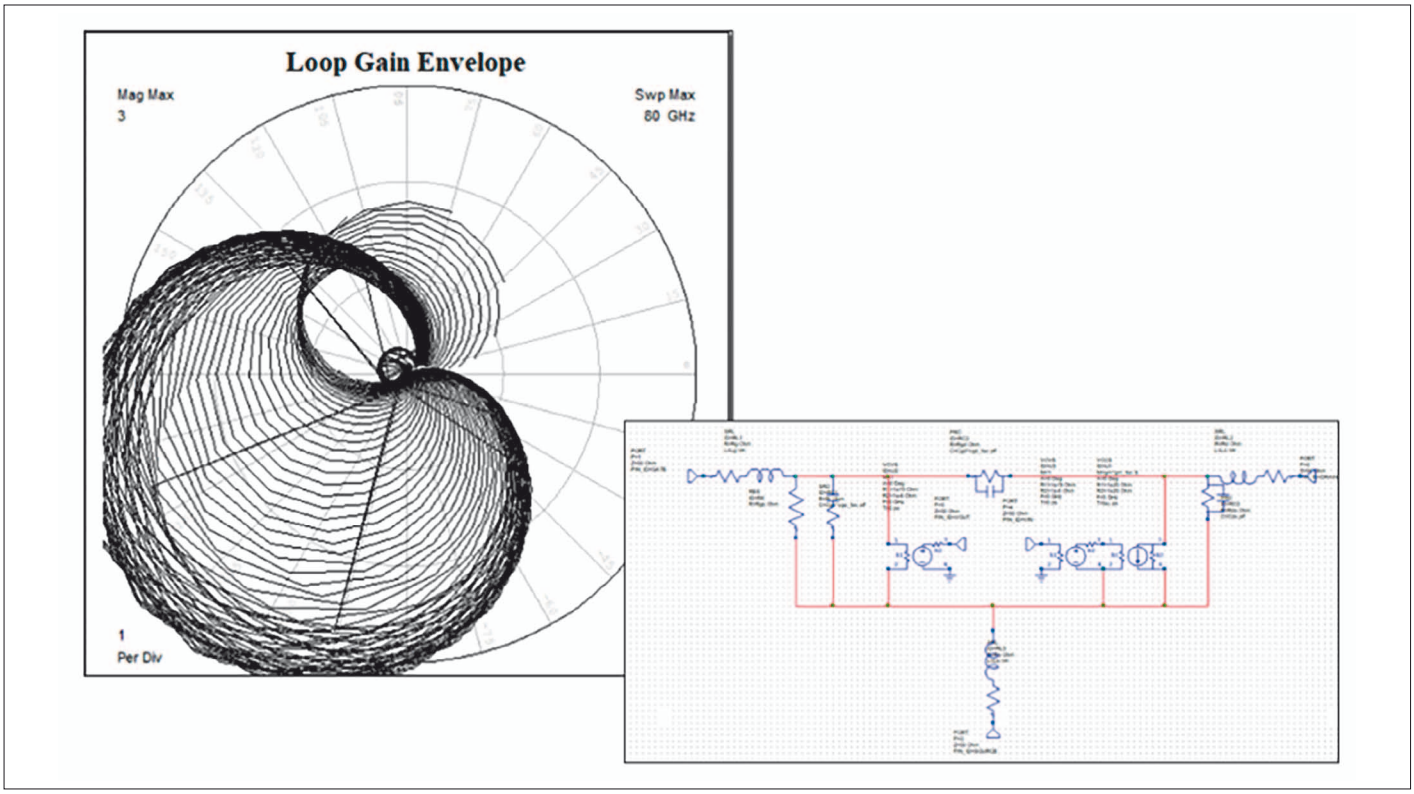
Several key new enhancements have been introduced to the meshing and solver technology in the AXIEM simulator to enhance the speed and capacity of EM analysis for MMICs and RFICs, as well as package and board structures. The latest via meshing technology provides robust healing to reduce mesh size (the overall number of unknowns) in multi-layer PCB designs and MMICs (Figure above).

Complex PCB and SoC components contain manufacturing features that do not impact RF performance yet slow down EM analysis by unnecessarily increasing the problem size. Shape pre-processing rules have been expanded in the AWR Design Environment V15 software to better address Si processes such as handling large numbers of metal layers by merging via arrays on user-specified layers and inside/outside a specified region. In addition, enhancements to the AXIEM DC solver (used for characterizing low frequency behavior such as bias networks) include new sparse symmetric matrix technology that provides at least a 10-fold savings in time and memory usage.

Related to these types of structures, the layer process definition file (LPF) in Microwave Office software defines the processing layers and parameters for the physical layout design. The AWR Design Environment has always offered multiple process definitions within a single hierarchical project to support analysis of heterogeneous substrates and multi-chip modules utilizing different semiconductor processes and laminates. The latest AWR Design Environment V15 release now supports "per-process technology" native LPF units, allowing different processes to specify units (mils or microns) that are most appropriate for a given technology.

More Design Power for the PA Designer

Stability analysis is critical to PA design and optimization. The commonly used K and μ-factors, derived from linear circuit simulation, can accurately predict whether a two-port network is unconditionally stable, yet they cannot detect insta-



Loop gain envelop results from amplifier stability analysis

bilities for multi-stage amplifiers or devices connected in parallel. Other stability analyses such as normalized determinate function (NDF) and loop gain techniques overcome these limitations but typically do so at the cost of computation run times, rendering them too slow for performing optimization.

The loop-gain envelope technique, a method for evaluating the envelope of traditional loop-gain stability circles, has been shown to cut the simulation time of this more rigorous approach to stability analysis from hours down to seconds, making it ideal for stability optimization [2]. The new AWR Design Environment V15 release now supports this method with a loop-gain envelope algorithm and equation block that can be easily applied to new amplifier designs.

The support for loop-gain envelope stability analysis offers designers several benefits. The stability and margin of stability of each device within a MMIC amplifier design is quantified. Analysis speed is increased by analytically applying the input and output terminations and, in addition, fewer N-phase combination evaluations are required, which also increases analysis speed. Due to the speed enhancements, optimization of phase margin for each device within a MMIC is now possible. The magnitude of source and load gamma are selectable, providing the MMIC designer with the ability to quickly determine stability into different loading conditions, as well as the ability to optimize to less stressful loading conditions for performance enhancement.

Baseband impedance variations over bandwidth in wideband PAs can impact device linearity, resulting in intermodulation distortion (IMD) levels that can vary asymmetrically with instantaneous signal bandwidth. This is associated with baseband memory effects [3] [4], which conventional PA design reduces by using video bypass capacitors to terminate the baseband impedance with short circuits.

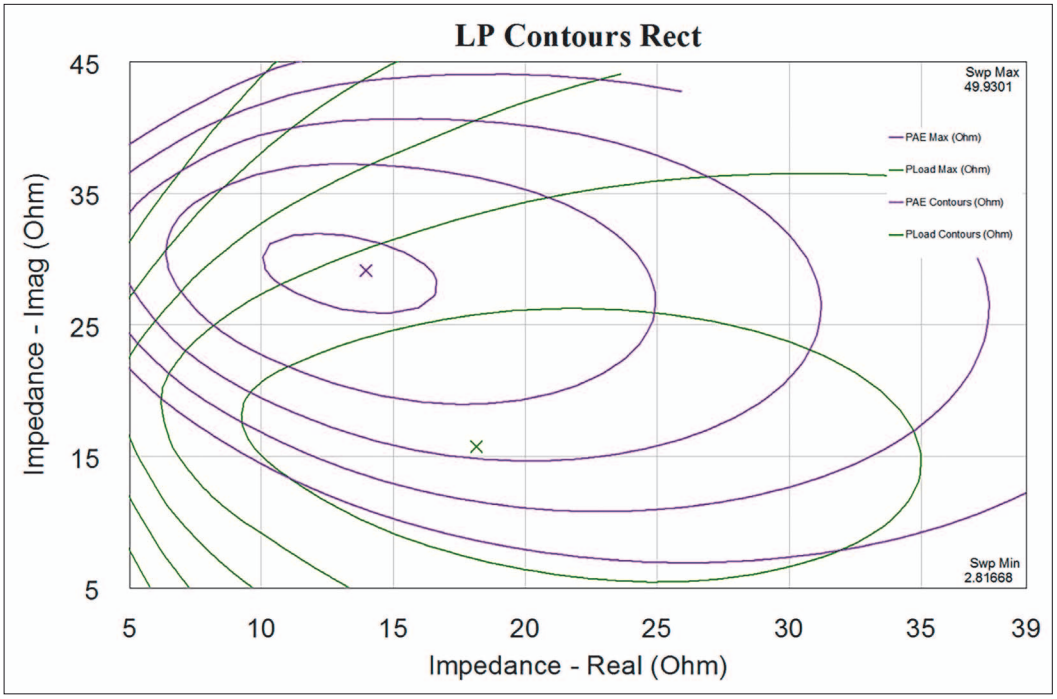
Performance can be improved by considering alternative baseband impedance conditions. PA developers have achieved significant improvements in linearity when active, baseband injection architectures such as envelope tracking (ET) are employed [5]. The AWR Design Environment V15 release enables designers to optimize PA linearity performance through video band load-pull analysis, which supports impedance tuning at the 4th and 5th harmonics, as well as the ability to generate contours on rectangular plots for enhanced visualization of performance versus load impedance, shown in Figure 4. These new features join the existing best-in-class load-pull capabilities in AWR Microwave Office software as part of an optional advanced load-pull tool kit.

Synthesis Accelerates Designs

The characteristic impedance and electrical length (delay) of transmission lines represent two important design parameters used to control the frequency-dependent circuit response of passive RF/microwave circuits such as quarter-wave impedance transformers, Wilkinson power dividers/combiners, hybrid couplers, filters and more. In the AWR Design Environment V15 software, designers can directly synthesize the physical attributes (width, length) of these microstrip, stripline, or co-planar waveguide structures for a given substrate based on the desired electrical characteristics.

Likewise, the electrical characteristics can be calculated directly from the physical properties of a single or edge-coupled transmission line placed in the schematic. Synthesis of circuit model parameters provides vital data for generating accurate layout of these transmission lines without manually invoking the TX-LINE calculator and transferring the results into the transmission line property dialog box.

Further expanding synthesis as a powerful design utility, the latest version of the Microwave Office network synthesis wizard expedites impedance-matching network development by allowing users to directly generate a matching network using components from the Microwave Office



Load-pull performance contours plotted on a rectangular grid in the AWR Design Environment V15 release of Microwave Office software

vendor library for surface-mount PCB-based designs. This capability also supports models from process design kits (PDKs), thereby extending the matching-circuit synthesis feature to include MMIC PAs and other MMIC-based designs.

Summary

The Cadence AWR Design Environment V15 brings RF/microwave design solutions for MMIC, PCB, and small-scale RFIC front-end blocks to Cadence's portfolio of EDA software solutions. These new capabilities address stability analysis, video band (and 4th and 5th harmonic) load-pull analysis, and improved harmonic balance (HB) simulation and performance. All stages of design are accelerated with the latest enhancements to network synthesis that support the incorporation of vendor components directly into a synthesized matching circuit, single and coupled transmission line synthesis, and faster planar EM meshing/solver technology targeting Si and PCB designs.

Furthermore, the Cadence Intelligent System Design strategy aligns with a future in which electronic design is multi-faceted and reliant on multi-physics and a host of design disciplines, with integrated RF/microwave content as a common factor. The microwave/mmWave technology and development tools called for in the 1980's MIMIC program has evolved to a level of complexity few could have imagined. And yet, "More than Moore" growth is exploding through tool development and collaboration that are well-aligned with the original vision of this program and are now serving 5G and other next-generation wireless systems.

References

[1] D. Vye, "How Design Software Changed the World, Part I," Microwave Journal, Jul. 1, 2009.

[2] M. Roberg, „Loop Gain Envelope Evaluation for Rapid MMIC Amplifier Stability Analysis," in IEEE Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS), Waco, TX, 2019, pp. 1-4.

[3] Joel Vuolevi and Timo Rahkonen, "Distortion in RF Power Amplifiers," Norwood, MA: Artech House, 2003.

[4] J. Vuolevi, J. Manninen, and T. Rahkonen, "Cancelling the Memory Effects in RF Power Amplifiers," IEEE Int. Symp. Circuits and Systems, 2001, pp. 57–60.

[5] Akmal, M., Lees, J., Ben Smida, S., Woodington, S., Carrubba, V., Cripps, S., ... Tasker, P. J., "The Effect of Baseband Impedance Termination on the Linearity of GaN HEMTs," European Microwave Conference, 2010, pp. 1046-1049. ◀