Design Challenges of Next-Generation AESA Radar

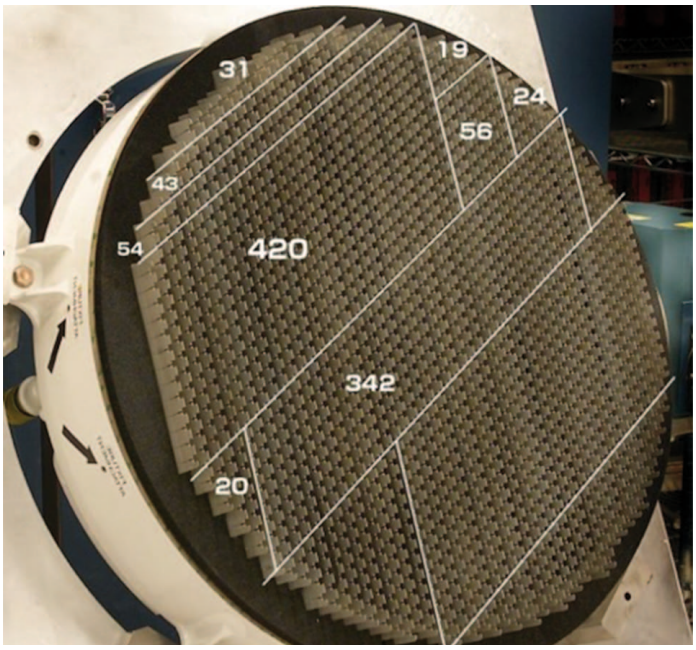

Figure 1: AN/APG-80 F-16 AESA radar from Northrup Grumman showing partial (half) count of individual array elements.

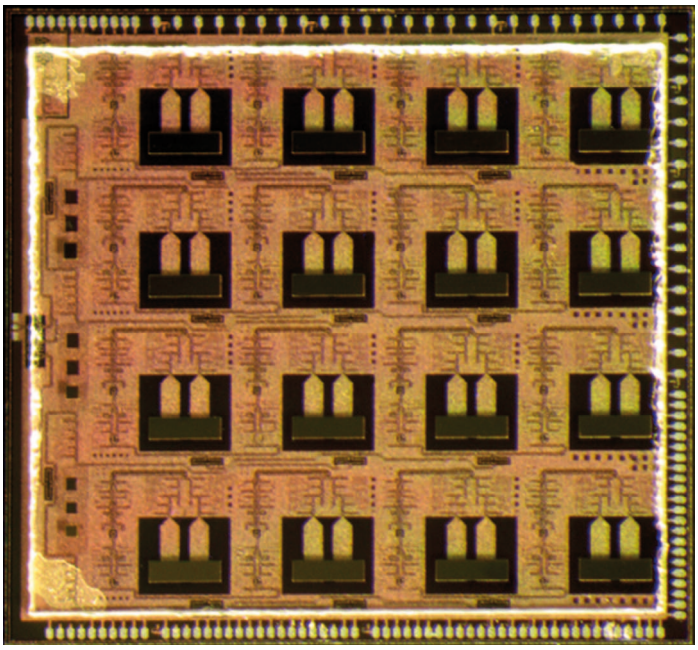

Figure 2: 4x4 wafer-scale phased-array transmitter at 110 GHz.

This article examines technology trends and presents several examples where advances in NI AWR Design Environment software are supporting next-generation AESA and phased-array radar development.

Phased-array antennas were first used in military radar systems to scan the radar beam quickly across the sky to detect planes and missiles. These systems are becoming popular for a variety of applications and new active electronically-scanned arrays (AESAs) are being used for radar systems in satellites and unmanned aerial vehicles. As these systems are deployed in new and novel ways, size and performance requirements are becoming critical and are being addressed through innovative architectures and system capabilities made possible through improvements in microwave and signal processing technologies such as GaN power amplifiers (PAs), new MMIC/Extreme MMIC devices, heterogeneous More-than-Moore integration, cost reductions for transmit/receive (T/R) modules, new mmWave silicon ICs, and electro-optic integration.[1]

To support these development efforts, electronic design automation (EDA) technologies are evolving to provide designers with system architecture, component specifications, physical design of individual components, and verification prior to prototyping.

Phased-Array Technology

An AESA-based radar, also known as active phased-array radar (APAR), consists of individual radiating elements (antennas), each with a T/R solid-state module containing a low-noise receiver, PA, and digitally-controlled phase/delay and gain elements. Phase and amplitude control of the input signal to the individual elements provides steerable directivity of the antenna beam over both azimuth and elevation, which allows the radar to aim the main lobe of the antenna in the desired direction. Unlike a mechanically steered radar, a phased array can rotate its pattern in space with practically no delay. Digital control of the module transmit/receive gain and timing permits the design of an antenna with not only beam steering agility and interleaving radar modes, but also extremely low side lobes, which provides a significant reduction in antenna radar signature compared to passive ESA and mechanically steered antennas.[2]

The width of the beam depends on the number of elements in the array. By increasing the number of elements (or sensors) in an array, the beam becomes sharper and thus more efficient in detecting smaller size targets. Today's AESA radars typically consist of thousands of individual elements electrically interconnected through increasingly complex structures designed for reduced size and weight, as well as increased performance (in other words, lower loss).

At lower RF frequencies (<10 GHz), where a longer wavelength increases the antenna size and spacing, the RF, intermediate frequency (IF), and/or baseband signal routing can be addressed with discrete components and off-the-shelf MMICs on printed circuit boards (PCBs)/packaging. The impact of longer traces will be offset by the lower PCB losses at these frequencies and the interface to the antenna can be considered independent of the IC unit cell due to the relatively flexible packaging requirements.

NI AWR
www.awr.com
www.ni.com

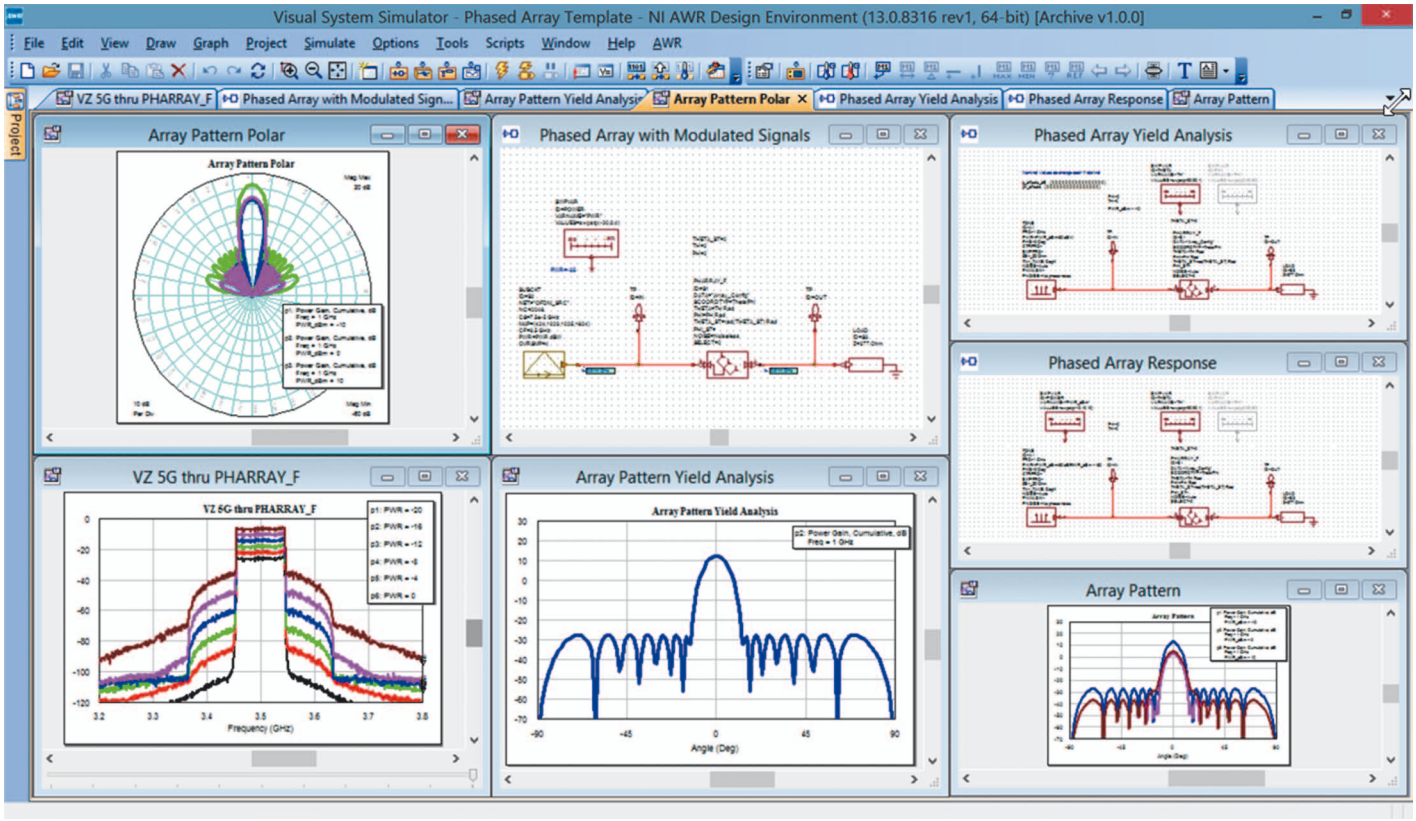

Figure 3: VSS phased-array modeling captures radiated power as a function of feed power levels, RF link budget and modulated waveforms used in communication systems.

However, at mmWave frequencies (>30 GHz), physically short antenna spacings (~wavelenth/2 < 5 mm), packaging losses, and manufacturing challenges with impedance-controlled multilayer packaging interconnects make high-functionality ICs and sophisticated integration schemes more attractive. Designing these types of complex packaging schemes for high-frequency signaling must be addressed with circuit simulation and EM analysis specialized for RF and microwave electronics.[3]

Evolving Integration Technology

While actively-steered phased-array antennas have many advantages, they are extremely complex and their production, especially non-recurring development costs, is significantly higher than conventional antenna design. These higher development costs are driven by the inclusion of hundreds to thousands of active electronic component modules per production unit, often implemented with custom gallium arsenide (GaAs) MMIC designs (typically five to 10 designs per system), as shown in Figure 1.

Initially funded and developed through Department of Defense (DoD) support in the 1980s and 1990s, GaAs MMIC technology was the only viable option for supporting the manufacture of the densely packed (cross section <1 cm) AESA T/R modules operating at 10...20 GHz. Advances in MMIC design have been enabled by the greater availability of powerful simulation software and inexpensive compute power, which enables engineers to design increasingly complex circuits with greater accuracy and to develop libraries of frequently used RF building blocks. Where earlier MMIC development addressed the challenge of combining tens to hundreds of active and passive components, including transistors, PIN diodes, resistors, capacitors, and inductors on a single GaAs substrate, integrating AESA functionality scales in complexity by combining radio blocks such as low-noise amplifiers, PAs, switching, and phase shifters onto a single or multi-channel MMIC. Even greater functionality/density levels are being developed through multi-chip modules (MCMs) utilizing revolutionary materials, devices, and advanced integration techniques.

The Defense Advanced Research Projects Agency (DARPA) Microsystems Technology Office has two programs investigating next-generation device integration. The DARPA Compound Semiconductor Materials on Silicon (COSMOS) program focused on developing new methods to tightly integrate compound semiconductor or III-V technologies within state-of-the-art silicon CMOS circuits. The DARPA Diverse Accessible Heterogeneous Integration (DAHI) program continues this work by developing heterogeneous integration processes to intimately combine advanced III-V devices, along with emerging materials and devices, with high-density silicon CMOS technology.[4]

Integration technology has made significant advances over the past 10 years. In 2006, Georgia Tech Research Institute developed a four- channel X-band SiGe T/R module with the control circuitry on a single chip for the DARPA Integrated Sensor is Structure (ISIS) program with a per-T/R module cost of about $10. In 2008, researchers at University of California San Diego (UCSD) enjoyed a huge leap in performance and integration density with the demonstration of the first RF-beamforming SiGe 6...18 GHz, 8-element phased-array receiver chip with 5-bit phase control and an on-chip 8:1 combiner.[5] UCSD followed up this work with a demonstration of the first 16-element 45...50 GHz phased-array transmitter in 2009. By 2013, a 110 GHz, 4x4 wafer-scale phased-array transmitter with high-efficiency on-chip antennas was reported by UCSD,[6] successfully demons-

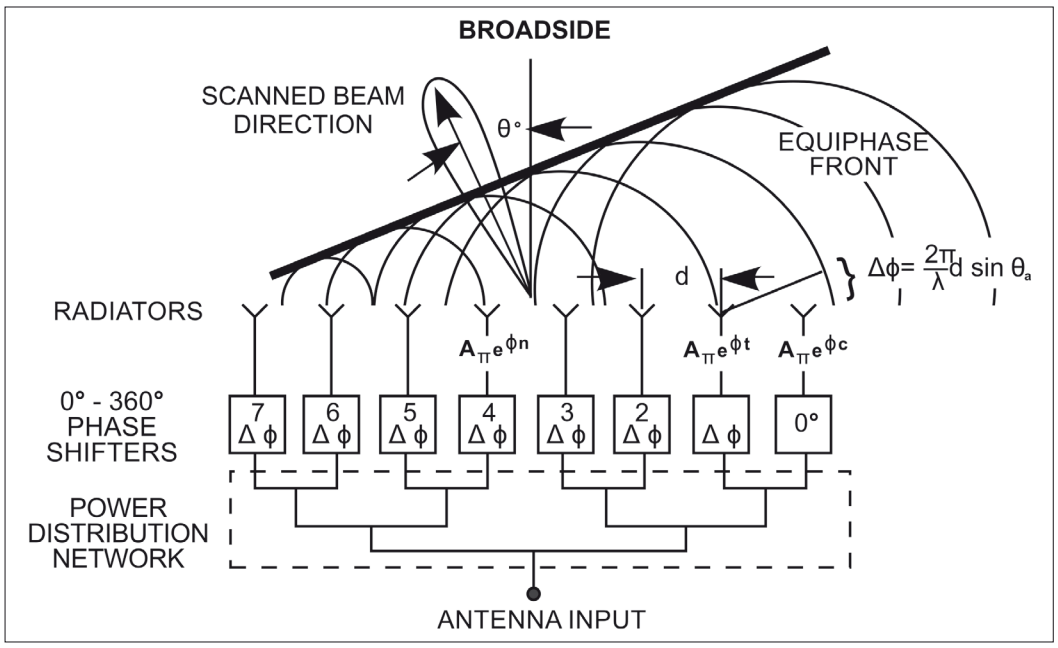

Figure 4. Gain tapering for beam shaping/steering and side lobe control.

trating a single chip solution, as shown in Figure 2.

Developments in GaN

While phased-array antennas are evolving into silicon core chips that support multiple radiating elements, preferred solutions frequently combine silicon with III-V front ends for applications that require the best possible performance, especially for figures of merit such as noise figure (NF) and output power. Increasingly, GaN is displacing GaAs as the material of choice for high-power or broadband front ends. For a fixed power level, a GaN MMIC can be one third to one quarter the size of an equivalent power GaAs MMIC, a power density that is enough to offset the higher material cost of GaN compared to GaAs. While the finished GaN wafer (including material) costs 2x that of GaAs, the resulting GaN solution is only 50-66 percent of the cost per RF watt generated with a GaAs solution. As the cost of GaN continues to decrease, the eventual elimination of GaAs from phased antennas could be expected for many applications.[7]

Continued investment in wide bandgap (WBG) semiconductors is expected to take More-than-Moore power electronics to another level. Researchers are looking to enhance GaN technology by heterogeneously integrating GaN on top of silicon wafers. The integration of GaN technology onto larger silicon wafers and use of standard semiconductor manufacturing processing will provide significant functionality and performance advantages at a much lower cost. All these technology options require that designers have an efficient way to understand tradeoffs between individual technologies and the impact on overall performance.

Even though the density of a GaAs MMIC is much lower than that of competitive silicon digital ICs, high-frequency electronic design requires careful attention to interconnect technology and EM-aware simulation that is able to predict the parasitic behavior that leads to performance failures. The physical arrangement or layout of components and interconnects is such a critical part of RF/microwave circuit design that NI AWR Design Environment utilizes a unified data model to inherently link schematic-based electrical elements to EM simulation-ready layout. This level of analysis is increasingly critical to successful MMIC development as the technology and integration levels evolve.

While the integration of III-V and silicon technologies addresses the size and functionality requirements of next-generation phased arrays, high density ICs also increase the need for wafer processing quality since losing one transistor out of a hundred due to a fabrication defect amounts to losing the entire (costly) die. As a result, the design of a complete microwave RF circuit on a chip will require established RF design rules for the layout of components and interconnections. In addition, robust design by way of yield/corner analysis must also be incorporated into the design stage in order to study the impact of manufacturing tolerances.

System Simulation for Phased Arrays

Design failure and the resulting high costs of development is often due in part to the inability of high-level system tools to accurately model the interactions between the multitude of electrically interconnected channels that are specified separately. Constructing full or partial phased-array systems to investigate these unforeseen interactions is also very expensive, both in terms of the expense of fabrication and the high cost to test the interactions of hundreds to thousands of channels. This challenge will only increase as the antenna-array and beam-steering control electronics continue along the current integration path.

With the design of such systems through fabrication and test iterations being cost prohibitive, development efforts are typically limited to one prototype in a Phase I or Phase II proof-of-concept demonstration. Failure to meet the specifications would lead to an unacceptable number of design and test iterations of the complete system (antenna/electronics). Therefore, simulation that incorporates the entire system has become a necessity. Since phased-array performance is neither driven purely by the antenna nor microwave electronics behavior, simulation must capture their combined interaction in order to accurately predict the overall system.

Oftentimes, high-level system analysis is performed using custom implementations by way of spreadsheets or generic mathematical calculations. Typically, these custom solutions vary in complexity from company to company and even between different projects within the same company. Such custom tools are generally used to specify the performance requirements of the underlying subsystems (MMICs/antennas/RF passives/control).

The more robust analysis offered by VSS communication system design software, combines the performance metrics of each of the subcomponents of a phased-array system to provide a more accurate accounting of the high-level system performance (Figure 3). Initially the analysis would be used to specify the overall system component topology and performance requirements on the individual subsystems. As more detailed models of the subsystems become available, these models and/or measurements of subsystems can be integrated into the full system analysis to obtain a better understanding of the overall system performance.

Phased-Array Antenna Features

Novel capabilities for full system analysis of actively-steered phased-array antennas are offered by VSS software. The simulator provides full system performance as a function of steered beam direction, the antenna design, and active and passive circuit elements used to implement the electronic beam steering.

System analysis enables designers to:

Evaluate array performance for over a range or power levels and/or frequencies

Perform budget analysis measurements such as cascaded gain, NF, P1dB, and gain-to-noise temperature (G/T)

Evaluate sensitivity to imperfections and hardware impairments via yield analysis

Perform end-to-end system simulations using a complete model of the phased array

In addition, parametric analysis allows the designer to efficiently study changes in the system design to balance cost versus system performance. Examples of parametric studies include T/R module specifications, phase-shifter errors (number of bits), combiner/divider topologies, resistive versus reactive amplitude shaping, the number of antenna elements, and antenna element spacing.

VSS software further offers phased-array simulation capability that enables modeling of phased arrays with thousands of antenna elements. It allows array configuration using various standards, as well as custom geometries. The phased array's behavior can be easily defined through the parameter dialog box or through a data le containing configuration parameters such as gain and phase offset, theta/phi angles of incidence, x/y location (length units or lambda-based) and signal frequency. The phased-array model can be set to either TX or RX modes. In TX mode, the signal power exciting each element is calculated based on the signal setting defined by the user with options that include:

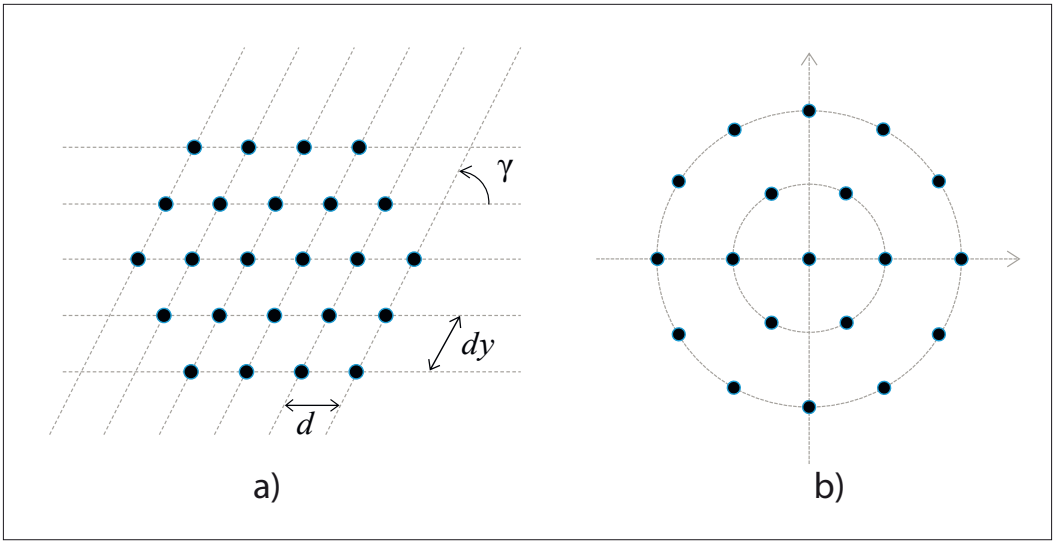

Figure 5: Standard array geometries for phased arrays in VSS – a) lattice, b) circular.

Lossless – excites all array elements by the power of the input signal

Power divider – the input signal is divided equally among all array elements

Voltage divider – the input signal is divided equally among all array elements such that the sum of their voltages equals the input signal

Control of the amplitude excitation through gain tapering is often used for beam shaping and to reduce the side lobe levels. A number of commonly used gain tapers are implemented in the phased-array block. Gain taper coefficient handling defines whether the gain taper is normalized or not. If it is, the taper is normalized to unit gain. Standard gain tapers implemented in the phased-array model include Dolph-Chebyshev, Taylor Hansen, and uniform. In addition, the user can de ne custom gain tapers by specifying the gains (dB) and phases for each array element, as shown in Figure 4.

Along with various signal distribution schemes and support for frequency-dependent operation, the model also allows the user to simulate array imperfections due to manufacturing flaws or element failure. All gain/phase calculations are performed internally, and yield analysis can be applied to the block in order to evaluate sensitivity to variances of any of the defining phased array parameters.

The parameter dialog box enables the user to quickly de ne an antenna-array architecture using standard or custom geometries. The lattice option allows configuration of the phased array in a lattice pattern using the number of elements along the x and y axes, nx and ny, element spacing along these axes, dx and dy, and gamma, the angle between these axes. Setting gamma to 90 degrees results in a rectangular lattice, while setting it to 60° creates a triangular lattice.

Any positive value for gamma may be used to configure the lattice while the circular option enables configuration of circular phased arrays with one or more concentric circles. The number of elements in each concentric circle and the radius of each circle can be defined as vectors by variables nc and r. Examples of lattice and circular array configurations are shown in Figure 5. Alternately, the user-defined option allows for custom array architectures, using the number of array elements, n, and their x/y locations.

Designers can de ne gains or full radiation patterns for each antenna element (Figure 6) in the phased array. This enables them to use different radiation patterns for internal, edge, and corner elements of the phased array. The radiation pattern of each antenna element will often be affected by its position in the phase array. These patterns can be measured in the lab or calculated in the integrated AXIEM planar 3D and Analyst 3D FEM EM simulators. A simple approach is to use a 3x3 phased array and excite one element – either the internal element, one of the edge elements, or one of the corner elements – while terminating all others. This will provide the internal, edge, and corner element radiation patterns, which can then be automatically stored in data sets using NI AWR Design Environment output data measurements. This approach includes the effect of mutual coupling from first-order neighbors. A 5x5 element array may also be used to extend mutual coupling to first- and second-order neighbors.

RF Link Modeling

VSS software also boasts the capability to model the RF links of individual elements in the phased array. This is an important functionality since RF links are not ideal and can cause the array behavior to deviate significantly from its ideal one. As an example, gain tapers are com-

[1] www.ncbi.nlm.nih.gov/pmc/articles/PMC3928903/

[2] www.ausairpower.net/aesa-intro.html

[3] Xiaoxiong Gu et al., "W-Band Scalable Phased Arrays for Imaging and Communications," IEEE Commun. Mag., April 2011, pp. 196-20.

[4] Sanjay Raman et al., "The DARPA Diverse Accessible Heterogeneous Integration (DAHI) Program: Towards a Next-Generation Technology Platform for High-Performance Microsystems", CS MANTECH Conference, April 23rd - 26th, 2012, Boston, Massachusetts, USA

[5] www.microwavejournal.com/articles/4757-an-eight-element-6-to-18-ghz-sige-bicmos-rfic-phased-array-receiver

[6] http://phys.org/news/2012-04-silicon-wafer-scale-ghz-phased-array.html

[7] Mike Harris et al., "GaN-based Components for Transmit/Receive Modules in Active Electronically Scanned Arrays", CS MANTECH Conference, May 13th - 16th, 2013, New Orleans, Louisiana, USA

[8] www.nssl.noaa.gov/publications/mpar_reports/LMCO_Consult2.pdf

monly used in phased arrays; however, when identical RF links are used for all antenna elements, this may cause certain elements (the ones with higher gains) to operate near or in compression while others in pure linear region. In this case, the array performance will be significantly impacted by how close to compression the elements are operating. Alternatively, based on the gain tapers that are used, designers may choose to use different RF link designs for different elements. While this is a more complicated task, it will result in more efficient phased arrays. VSS phased-array modeling allows designers to achieve uniform RF link design to all elements or at least account for the performance degradation from uneven RF links to each element. Being able to predict such performance and modify the RF designs so that requirements are met is one of the unique capabilities that the VSS phased-array modeling functionality offers.

Conclusion

As AESA radar systems become more sophisticated with increased element counts and antenna/electronics integration advances, the capability to design and verify the performance of the individual components along with the entire signal channel is becoming critical. NI AWR software provides circuit simulation, system-level behavioral modeling, and EM analysis operating within a single platform enabling development teams to investigate system performance and component-to-component interaction prior to costly prototyping.

Radar technology, driven by new commercial and aerospace/defense applications, is enabled by evolving semiconductor, phased array, and integration technologies. EDA simulation software provides the necessary support for engineers developing the hardware responsible for these data-intensive, wireless sensors. As the underlying RF front-end technology and digital signal processing continue to grow more complex, RF-aware system simulation, inclusive of nonlinear RF circuit and EM antenna analysis, plays a critical role in the physical realization of these beam-steering and MIMO-based radar systems. NI AWR software includes all of the modeling and simulation technologies designers need to meet the challenges of all types of radar system design. To learn more about the breadth of products available for radar design, visit awr.com/radar. ◄

Signal Quality Analyzer Supports Receiver Test

Anritsu Corporation is pleased to announce the start of sales of its USB4 receiver test solution using the company's Signal Quality Analyzer-R MP1900A in combination with automation software from Granite River Labs or Teledyne LeCroy to control a connected oscilloscope and implement tests meeting the latest USB4 standards.

The spread of next generation 5G mobile communications and Internet of Things (IoT) devices is driving development of various new communications and IoT services that are massively increasing data volumes. To increase the speed of interfaces handling these large video and data files, smartphones, tablet PCs, and other digital devices are adopting USB Type-C connectors. These connectors are an extension of the USB 3.2 high-speed standard (10 Gbit/s x 2 lanes), which has now been extended again to USB4 offering doubled speeds of 20 Gbit/s x 2 lanes; USB4 compliance tests are being run in 2020. Due to

the 20-Gbit/s speed of USB4, the Electrical test places heavy emphasis on the Tr/Tf and intrinsic jitter performance of the test signal source because measurement-system noise and jitter cannot be ignored. Additionally, like previous USB tests, to assure accurate measurement of device receiver sensitivity, the test is performed by calibrating the test signal according to the minimum input performance defined by the receiver standards.

Automation of the BERT and oscilloscope combination is necessary to minimize the workload of signal calibration and optimize test reproducibility. The Signal Quality Analyzer-R MP1900A is a high-performance BERT supporting not only USB tests, but also receiver tests of high-speed computing and data communications interfaces, such as PCI Express, Thunderbolt and 400/800 GbE.

Its high-quality data output performance (12 ps t_r/t_f, and 115 fs rms Intrinsic Jitter) helps assure more accurate measurement of high-speed USB performance as required by the USB4 receiver test. In addition, combination with Granite River Labs GRL-USB4-RXA or Teledyne LeCroy QPHY-USB4-TX-RX (USB4/TBT3 transmitter and receiver) automation software for automating signal calibration and testing helps high-reproducibility measurement of USB4 interfaces according to the latest standards while also reducing test workload.

■ *Anritsu Corporation*
www.anritsu.com