Leveraging EM Analysis:

K-Band Satcom GaN HPA Design

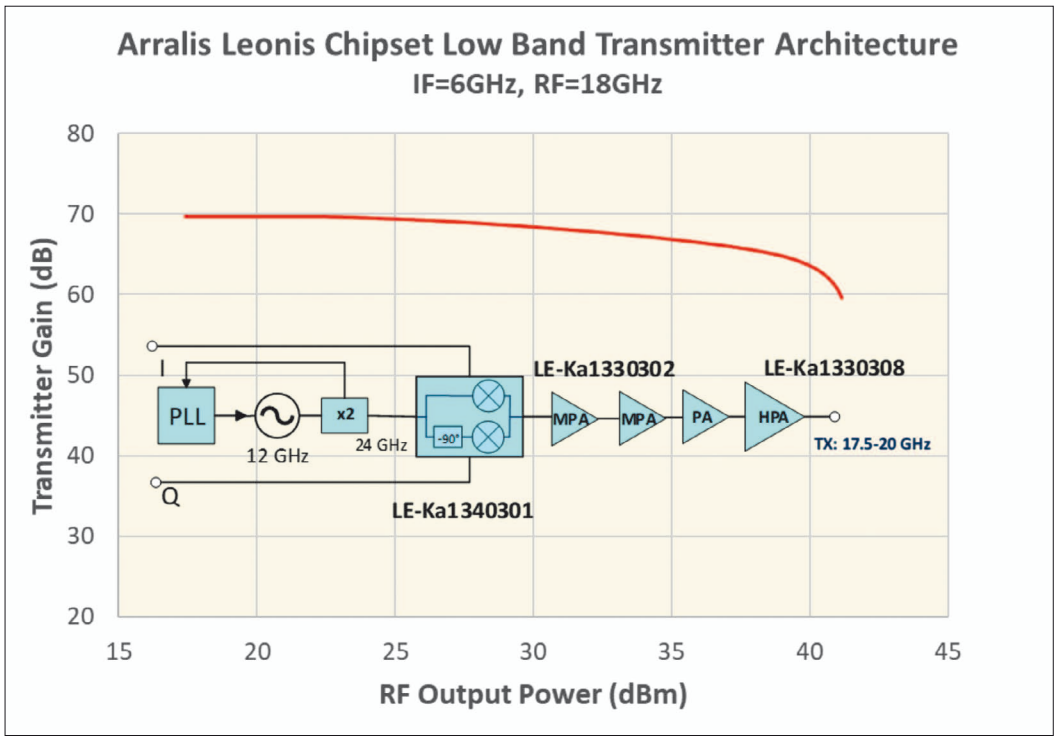

Figure 1: Arralis Leonis chipset for low-cost K/Ka-band satcom applications

K/Ka-band satellite communications (satcom) can provide constant, uninterrupted access to information, driving companies like Facebook, Amazon, Inmarsat, and SpaceX to invest heavily in this spectrum for global broadband services.

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SpaceX, for example, currently has plans to deliver Ka-band payloads across a constellation of 4,425 satellites. These systems are enabled through high-power amplifiers (HPAs), which form the final link in the RF power chain of next generation, satellite-based, RF front-end components. The Leonis chipset from Arralis Ltd (Limerick, Ireland), initially developed as part of the European Space Agency (ESA) ARTES program, addresses the growing demand for lower cost K/Ka-band satellite equipment.

The chipset includes mixers (IQ and sub-harmonic), up and downconverter core chips, switches, phase shifters, low-noise amplifiers (LNAs), and PAs. Within this chipset, the company's LE-Ka1330308 is a high-power monolithic microwave integrated circuit (MMIC) amplifier fabricated on space qualified 0.25 µm gallium nitride on silicon carbide (GaN on SiC).

Arralis successfully demonstrated transceiver architectures for both uplink and downlink communications. Figure 1 illustrates the low-band transmitter architecture and performance with the integrated HPA.

GaN MMIC Technology

Through the use of GaN technology, Arralis offers higher efficiencies, power density, and thermal conductivity compared with equivalent gallium arsenide (GaAs) parts. In addition, GaN can operate at higher temperatures without loss of reliability, making it especially well-suited for satellite communications. Device thermography measurements of the die show a thermal resistance of 2.62 °C/W, resulting in a lifetime estimate of 5^7 hours.

The LE-Ka1330308 operates from 17.5 to 20 GHz and typically delivers 10 W saturated output power, with power-added efficiency of 25 % and large-signal gain of 20 dB in a compact die size of 3.7 x 3 mm (Figure 2). The three-stage MMIC amplifier, which is fabricated on the United Monolithic Semiconductors (UMS) International Traffic in Arms Regulations (ITAR)-free, space-qualified 0.25 µm GH25-10 GaN on SiC process, is matched to 50 ohms with integrated DC blocking capacitors on RF ports and incorporates an output power detector to assist with system integration.

During the design phase, extensive circuit design and simulation was performed using the NI AWR Design Environment platform, specifically Microwave Office circuit design software, AXIEM EM simulator for 3D planar structures (MMIC manifold feed network, on-chip passives, and PCB evaluation board), and Analyst EM simulator for 3D EM analysis of the package. The simulation software works with the active and passive MMIC component models developed by the foundry and organized into process design kits (PDKs) developed through collaboration between the NI and UMS modeling teams (refer to sidebar and Figure 6).

The MMIC die was represented in simulation using foundry-verified, schematic-based models and EM analysis, allowing the designers to reliably predict and optimize key performance metrics. Figure 3 shows the correlation between measured and modeled S-parameters. The graph also shows the simulated gain variation due to process tolerances. Measured gain performance falls on the high side of the variation, however it is within the predicted limits of the simulation.

Significant EM analysis and design optimization was carried out at the component and subcircuit level to ensure that parasitics and inadvertent EM coupling between structures is incorporated into the simulation.

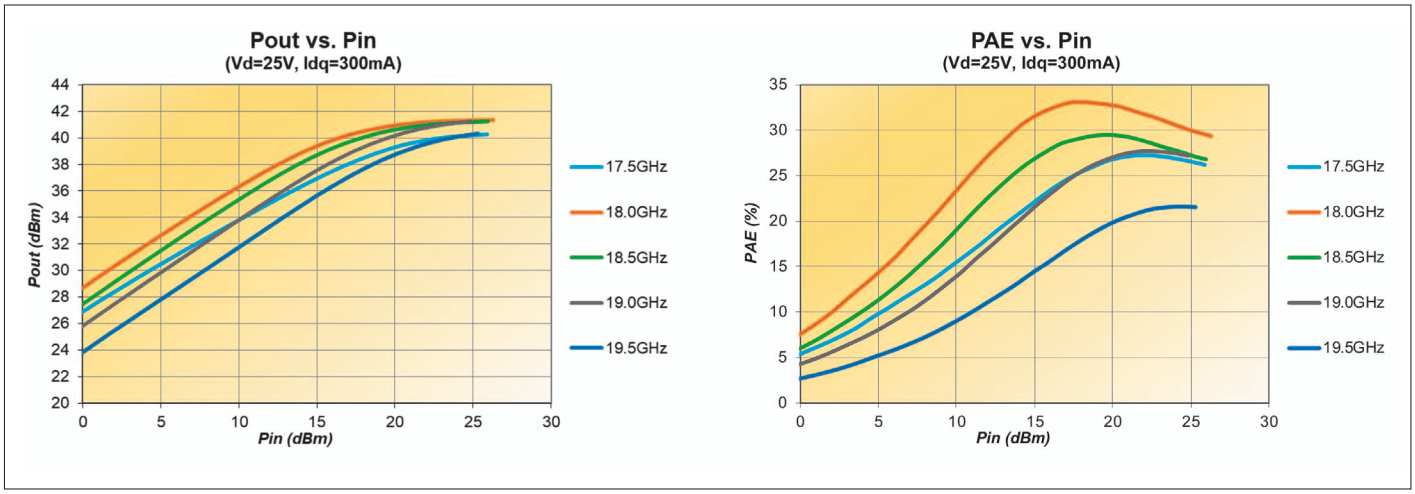

Figure 2: Output power (dBm) and PAE (%) as a function of input power over the 17.5 to 19.5 GHz range

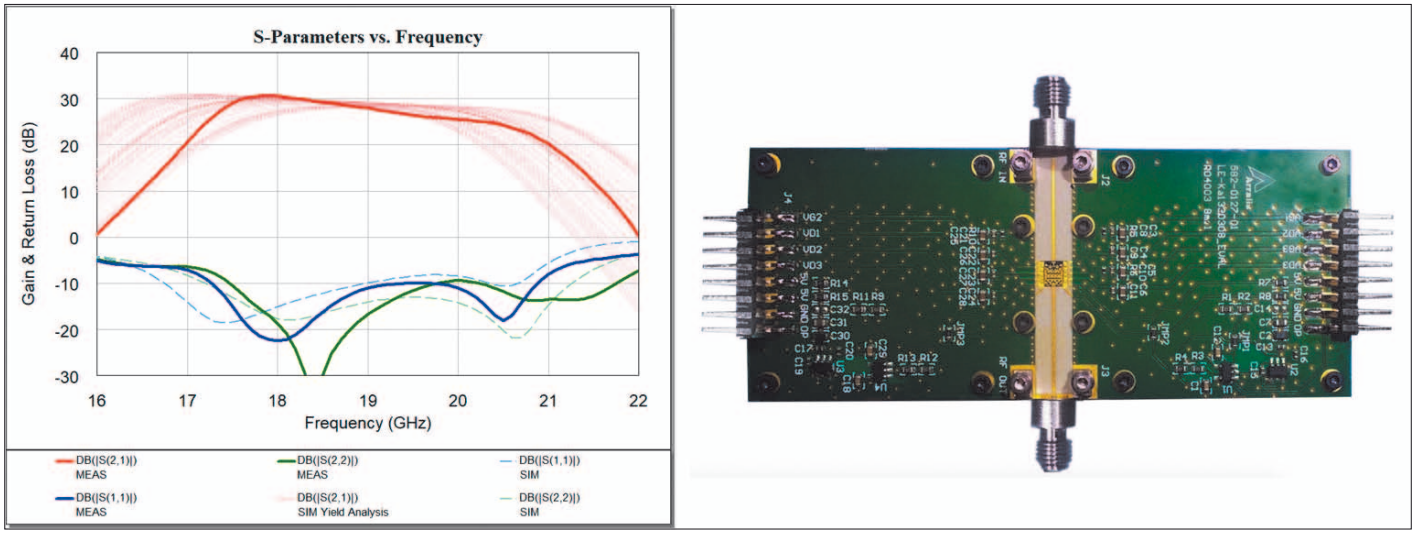

Figure 3: Simulated data including yield analysis vs. modeled small-signal frequency response for the LE-Ka1330308 reference board (right)

Towards the end of the design phase, larger and more integrated EM analysis was used as final verification and to ensure that all interactions were captured in simulation. These EM simulations were conducted using the AXIEM EM simulator.

The characterization and modeling methods implemented by the foundry have been validated through a well-established process/model qualification procedure, developed over years, that has been proven to yield reliable device models for the foundry's family of semiconductor processes. The extracted nonlinear models account for trapping phenomena and transistor self-heating. In addition to electrical characterization, the UMS modeling team performs a comprehensive study of the thermal device behavior and other non-stationary effects to improve the quality of its nonlinear device modeling.

Packaged Device

The success of the bare die MMIC has fuelled the subsequent development of a packaged part that will facilitate a more convenient solution for system integration. For best performance, a high thermal conductivity epoxy needs to be used and unwanted voiding eliminated. A packaged solution removes this delicate step for the customer while also providing an easy to handle part with integrated decoupling and wire bonding.

The Kyocera SGMR-B1193, a commercially available 7 x 7 mm ceramic quad-flat no-leads (QFN) package, was selected for investigation, as shown in Figure 4. This package will provide a hermetically sealed solution with enough space to accommodate the die and decoupling capa-

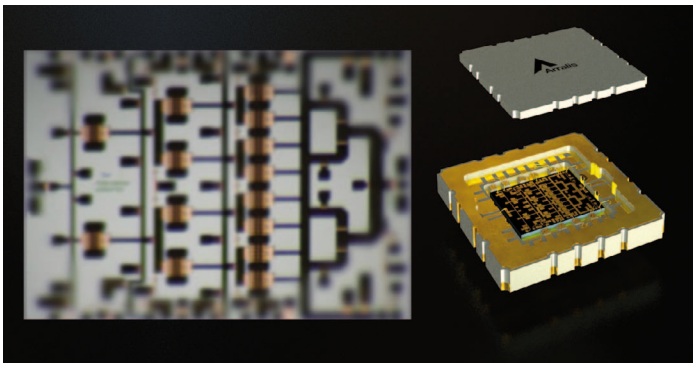

Figure 4: Proposed packaging (Kyocera SGMR-B1193) for K-band HPA. Image courtesy of Kyocera Corporation

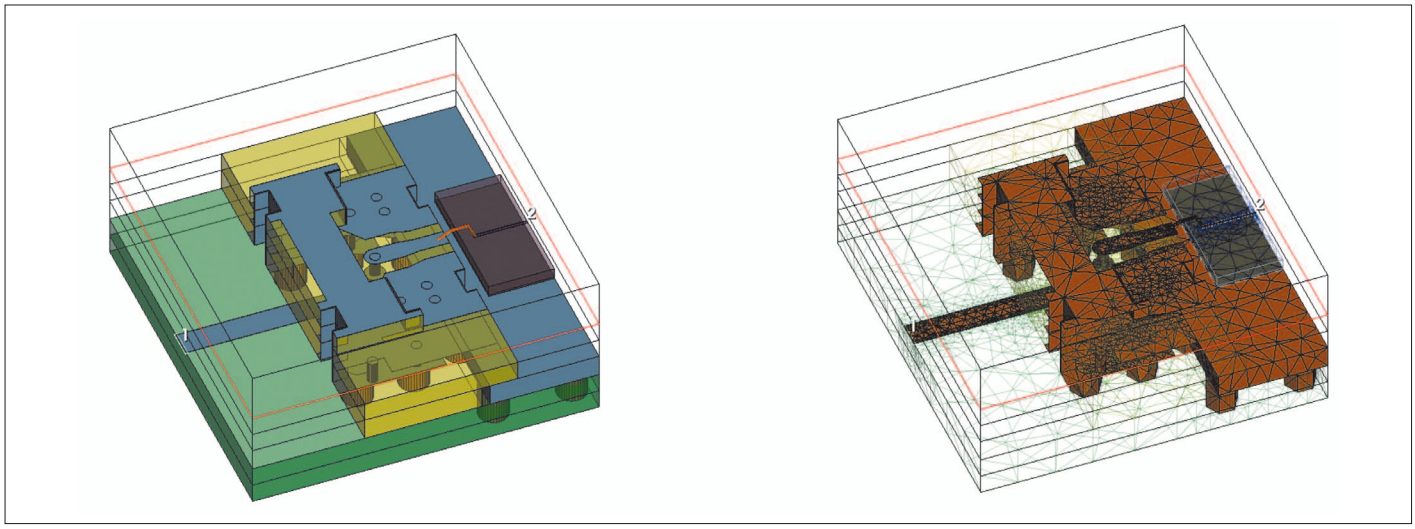

Figure 5: Details of package model I/O port simulation setup (left) and resulting mesh in Analyst software

citors, while also minimizing the RF I/O bond-wire length. A coefficients of thermal expansion (CTE)-matched MoCu heat sink will provide a reliable thermal path through the base. The ceramic QFN package is a compact size of 7 x 7 mm.

This RF transition has been simulated using the Analyst EM simulator (Figure 5) to minimize return loss due to impedance mismatches between the MMIC, the package, and the evaluation board.

The simulation results show a well-matched transition with insertion loss of 0.25 dB. This will translate to an overall gain reduction of 0.5 dB and power reduction of 0.25 dB for the packaged part compared to bare die option.

Conclusion

Arralis engineers have successfully designed a K/Ka-band chipset, inclusive of a 10 W saturated output power HPA, for satellite communications applications. The three-stage MMIC amplifier, fabricated with space-qualified, 0.25 µm GaN on SiC, was developed using state-of-the-art semiconductor technology, foundry-qualified device models, and NI AWR software circuit/EM simulation technology. Transceiver architectures for both uplink and downlink communications were demonstrated with this chipset and the integrated HPA. Additional development efforts are focused on integrating the bare die into a suitable package with initial samples of the packaged HPA, expected in early 2020. ◄

Process Design Kits (PDKs)

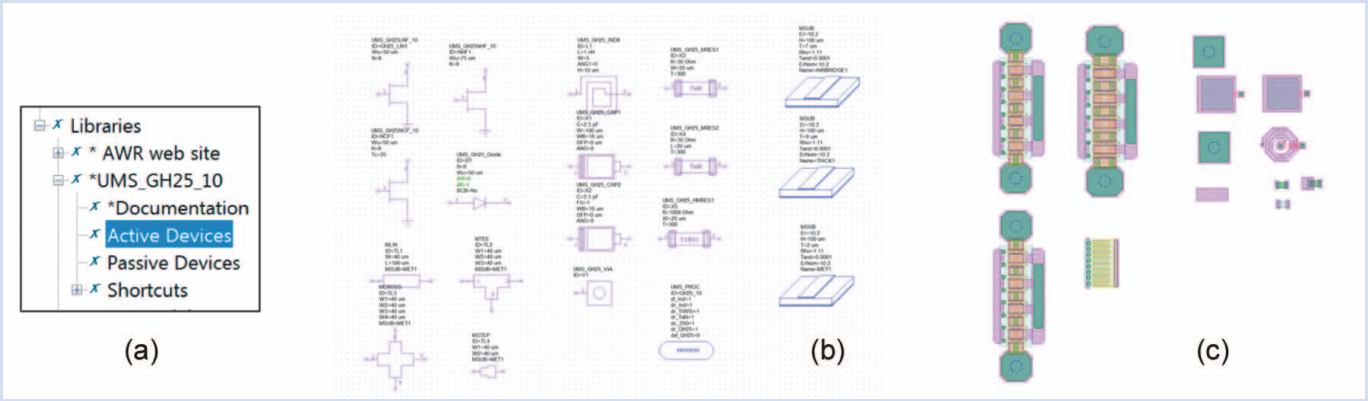

Figure 6: NI AWR software UMS PDK (a) element browser view, (b) schematic view, and (c) layout view

Active device models and passive on-chip components, along with their parametric layout cells (PCells), are organized into PDKs to support MMIC development. These PDKs provide simulation-ready device models to use in the construction of ICs for analysis and generation of layout masks for fabrication. The NI AWR software UMS GH25 PDK, available directly from the foundry, includes a layout process file (LPF), which defines the material stackup and metallization layers for EM simulation and physical realization of the MMIC. Select parameters of the active and passive device models, such as gate width/number of fingers or capacitor/inductor values, can be adjusted by the designer. In addition to PCells, models come with a symbol representation for schematic editing. Figure 6 shows the UMS GH25 PDK within the NI AWR software element browser, along with the corresponding schematic and layout views of various active and passive devices contained within the PDK. More information is available at www.ums-gaas.com/foundry/design-kits/.