Network Synthesis Wizard Automates Interactive Matching-Circuit Design

This application note highlights the network synthesis module within the NI AWR Design Environment platform, an electronic design automation (EDA) software technology that reduces design time in the domain of network synthesis by automating the development of impedance-matching circuits.

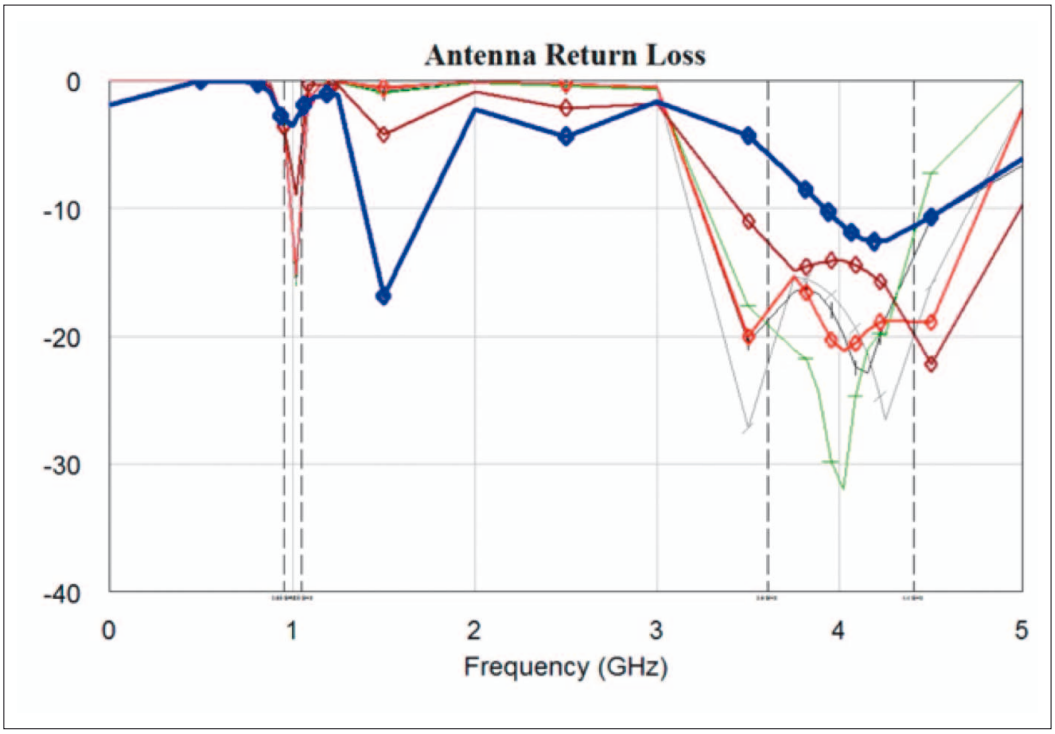

Figure 1: Network synthesis addresses multi-band matching challenges.

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Network synthesis technology is used for RF/microwave applications to ensure that the input impedance of an electrical load or the output impedance of its corresponding signal source maximizes the power transfer by minimizing signal reflection from the load that occurs from impedance mismatch.

Network synthesis is helpful at the earliest stages of a design to help determine reasonable performance targets based on device performance limits, device sizing (decisions on active device periphery), part selection for discrete packaged transistors, and other early design decisions.

Network Synthesis Wizard

The network synthesis wizard accelerates design starts and enables designers to more fully explore design options through the creation of optimized two-port matching networks with discrete and distributed components based on user-defined performance goals.

This synthesis solution is particularly helpful for challenging broadband single- and multi-stage amplifiers and antenna/amplifier matching networks

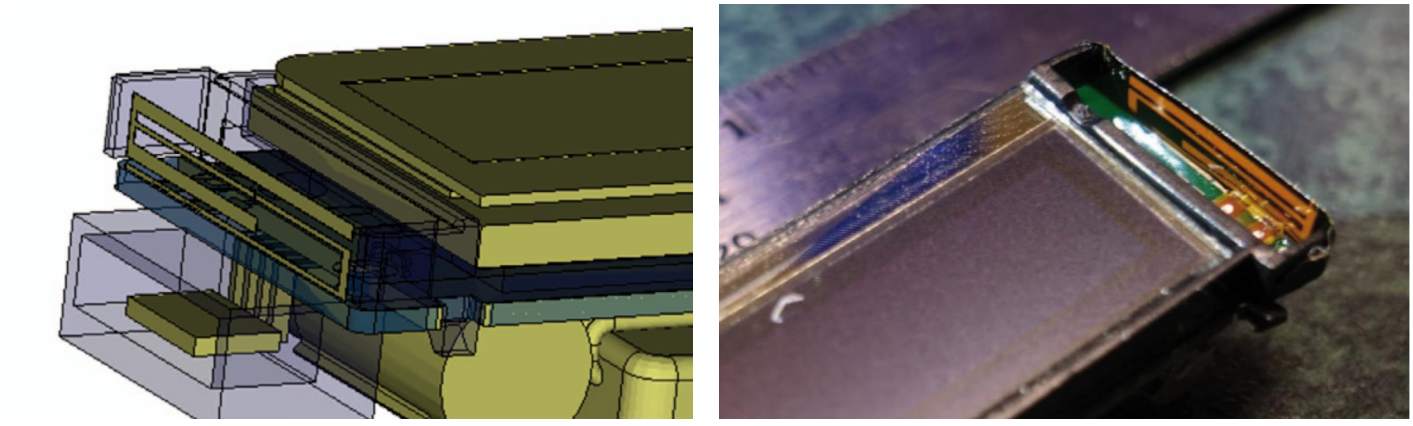

Figure 2: Embedded antenna and RF front-end in wireless wearable device (images courtesy of Striiv).

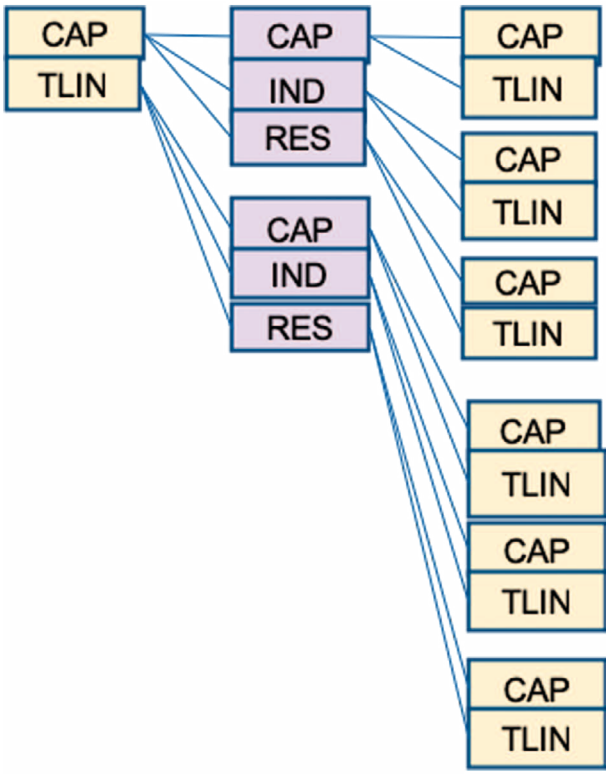

Figure 3: The search engine explores possible topologies by expanding the solution up to the maximum number of sections as defined by the user.

(Figure 1). The tool aids designers in developing impedance-matching networks between front-end components. As the footprints of RF components shrink, to meet market demand for smaller embedded radios in internet of things (IoT) smart devices (Figure 2), for example, the network synthesis wizard helps designers save space, consolidating component-to-component matching networks by directly transforming the impedance between each component rather than to an intermediary characteristic impedance (such as 50 ohms).

Furthermore, networks can be optimized for noise, power, or interstage matching. The optimum reflection coefficients are specified over frequency and can be provided in the form of load-pull data, network parameter data files, or circuit schematics. Specifications for network topology include series and shunt component types and maximum number of sections.

With a given set of user input specifications (performance requirements), the synthesis algorithm searches circuit topologies and optimizes component parameter values to generate candidate matching networks for power and low-noise amplifiers, as well as inter-stage and inter-component impedance-matching networks.

Optimization Technology

The network synthesis wizard is made possible with recent advances in computer processing power and the introduction of genetic algorithm methods. Network synthesis leverages the algorithms first employed within the NI AWR software AntSyn antenna design, synthesis, and optimization tool (awrcorp.com/antsyn) and, as such, results in a rigorous optimizer. The optimizers use recombination and selection to rapidly and robustly explore numerous points randomly distributed over the design space. This provides in a more efficient and faster approach to investigating design possibilities and identifying optimum solutions.

The method used by the search-based synthesis engine to determine candidate circuit topologies is based on input from the user-specification of which element type, such as capacitors, inductors, and transmission lines, is to be used in the series and shunt slots. The synthesis tool then performs an exhaustive search, exploring all possible topologies by expanding the solution up to a maximum number of sections as defined by the user, as shown in Figure 3.

Heuristic methods are used to determine what element can follow an existing element. Through this self-learning process, the synthesizer understands that certain elements, such as two different width transmission lines, can be placed serially to form a stepped-impedance transformer or a fully-distributed transmission line network for

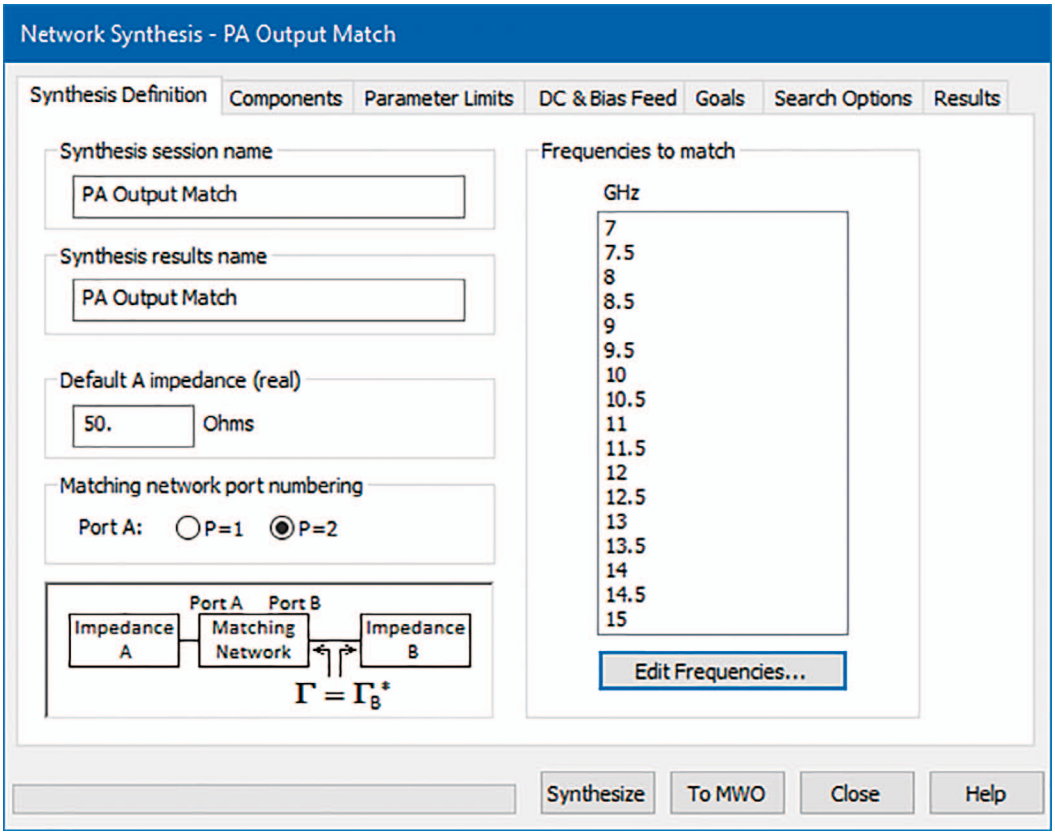

Figure 4: The synthesis definition dialog allows users to specify basic network parameters, including circuit location among networks to be matched, port numbering, and frequency band.

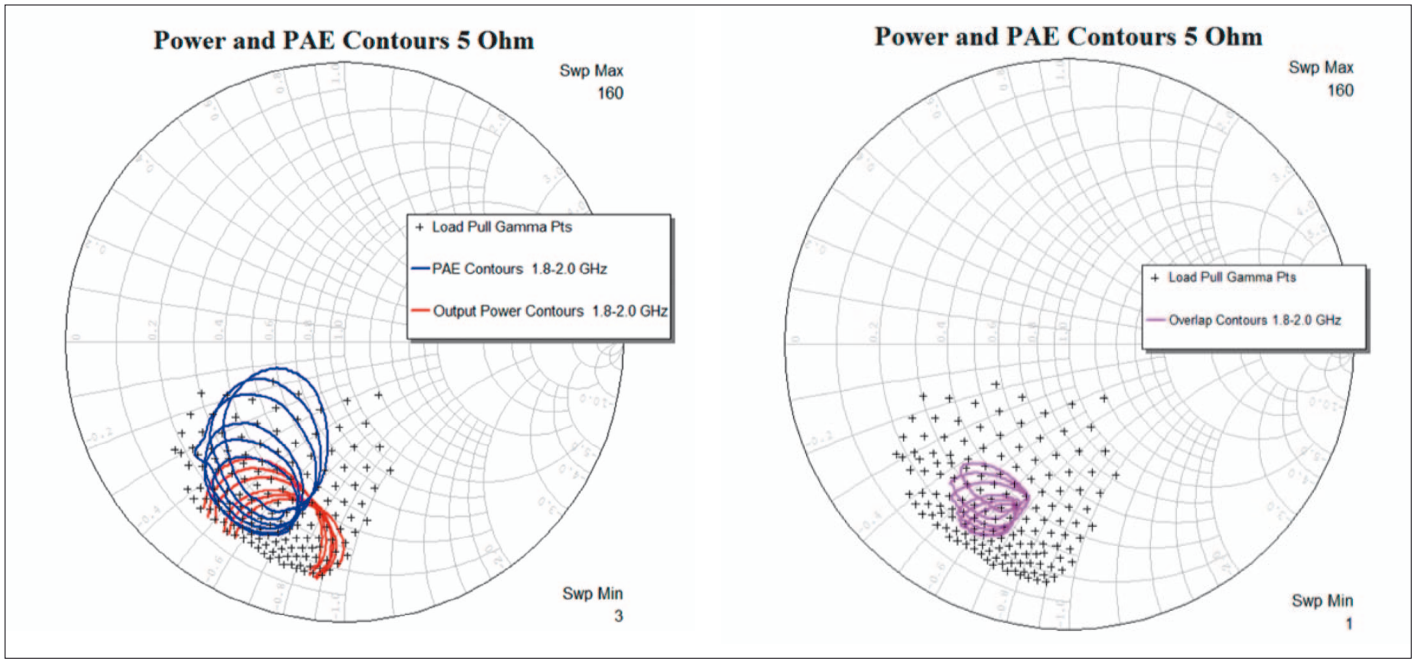

Figure 5: Load-pull contours for power and PAE (left), as well as the intersection of these contours (right).

higher frequencies. On the other hand, two serial capacitors would not make sense from a matching perspective, consequently, those search efforts are not pursued.

The optimization goals are specified in the wizard using a dedicated set of synthesis measurements. Specialized measurements are provided for input noise matching, amplifier output-power matching, and interstage matching. The optimum reflection coefficients are specified over frequency and can be provided in the form of load-pull data, network parameter-data files, or circuit schematics.

Additional practical considerations coded into the synthesizer include the ability to constrain the DC open and short paths in the topology search. For instance, the user can stipulate that the side of the matching circuit next to the device will be DC open, so as not to short the drain or collector. Users can also stipulate minimum and maximum component limits and discrete values to reflect actual available (discrete) parts as well as place constraints on the first and last components in the network. This constraint enables designers to ensure the physical practicality of the synthesized network, such as designing a wide (low impedance) transmission line termination adjacent to a large periphery device. In addition, the impact of pre-existing bias or feed networks can be incorporated into the synthesis network. The search results are then presented from best to worse (in addressing the performance goals) as each expansion is added.

Interactive User Interface

The network synthesis user interface (UI) lets designers inter-

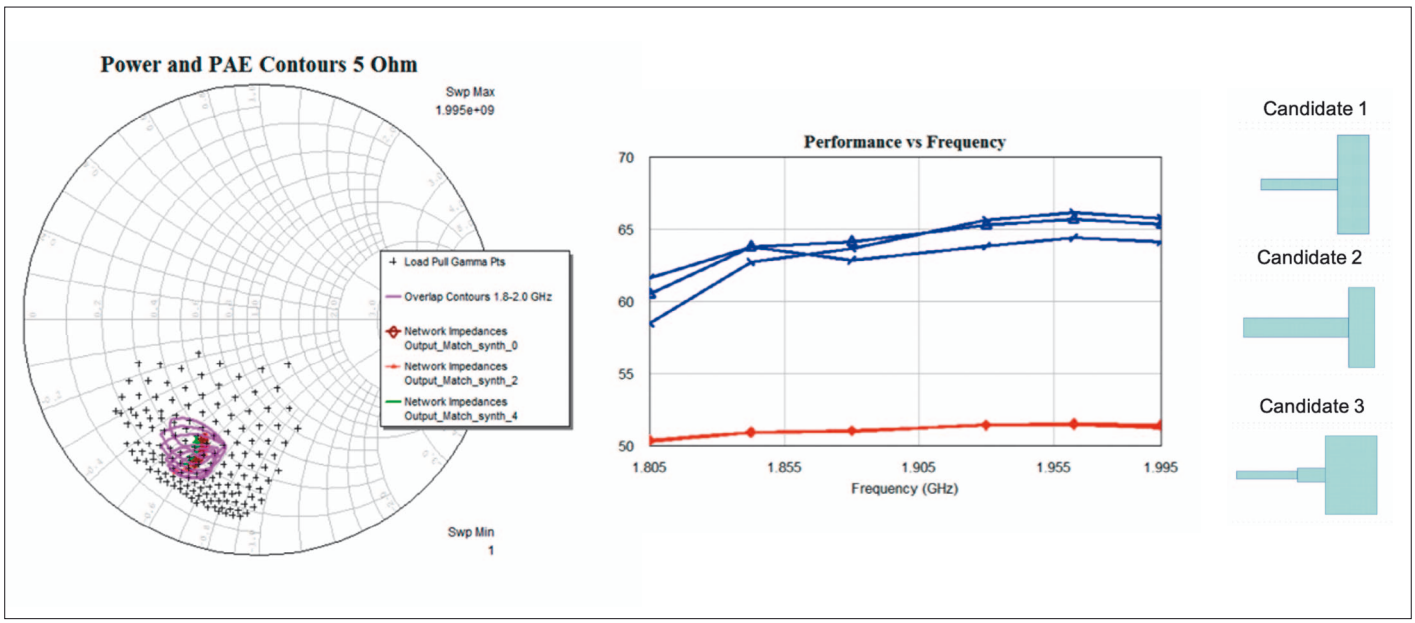

Figure 7: Candidate matching networks and corresponding performance provide users with a method to compare different results.

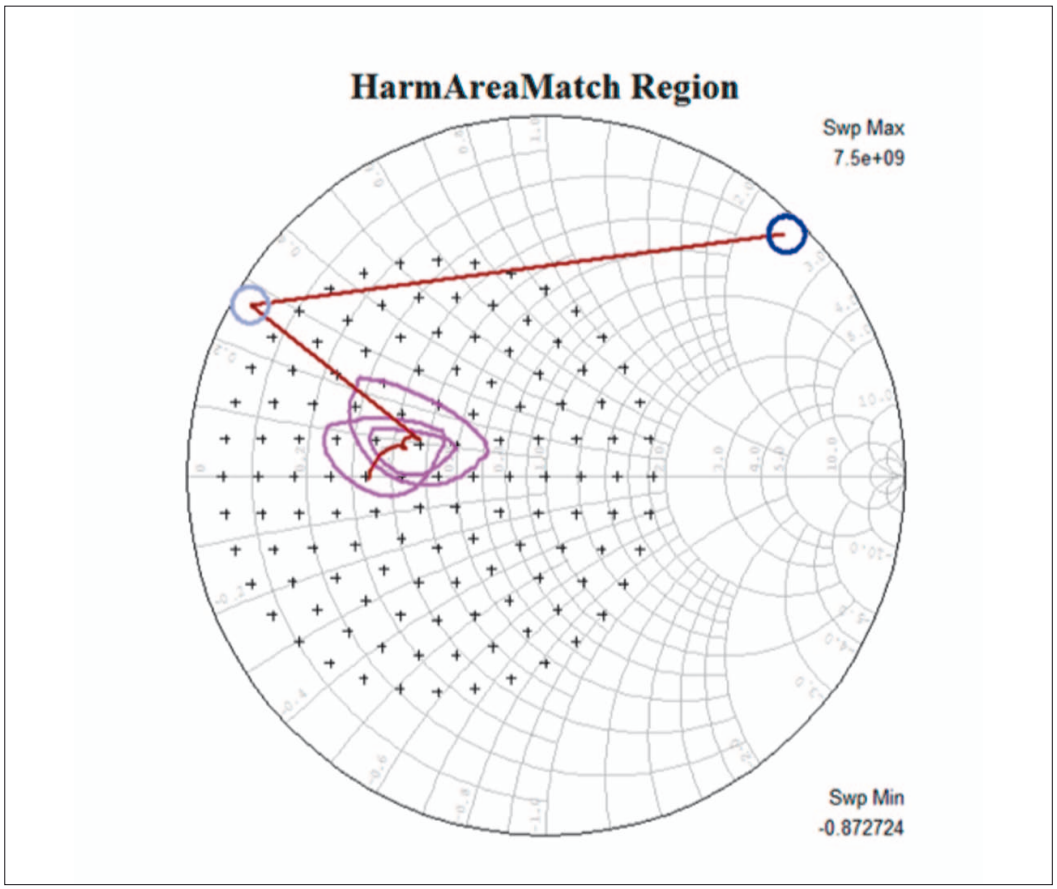

Figure 6: PAE/power overlap load-pull contours at three fundamental frequencies and user-defined additional goals for second and third harmonic terminations with resulting network synthesis generated matching circuit.

actively develop an unlimited number of networks optimized for noise, power, or matching networks between amplifier stages or between different components, such as an amplifier and antenna.

The optimum reflection coefficients are specified over frequency and can be provided in the form of load-pull data, network parameter data files, or circuit schematics. Within the synthesis definition tab (Figure 4), users can specify a default impedance or the impedance of the desired source/load network as well as the desired match frequencies.

The components tab lets users specify the two target networks to be matched from an automatically populated list of project networks (schematics), as well as a set certain of constraints on the matching network, including the number of sections, topology, component type, and configuration (series/shunt).

Valid topologies are determined by the types of components selected and the value specified for the maximum number of sections. Each section is either a series component or a shunt component. The wizard considers topologies having the maximum number of sections, such as N, and with fewer, down to N-3 sections, as previously noted.

An Example: Load Pull

The wizard interfaces directly with load-pull data within Microwave Office software for the instances where designers want to develop matching networks based on nonlinear, load-sensitive performance data. To illustrate, the locus of impedances resulting in power-added efficiency (PAE) and power contours over a given frequency range are plotted on a 5-ohm Smith chart (63% PAE and 1-dB power compression point at ~125 watts or 51 dBm, 5 frequencies from 1.8 to 2.0 GHz), as shown in Figure 5.

Alternatively, the designers could plot the overlapping contours, which represent the intersection of the PAE and 1 dB gain compression contours, as shown on the right side of Figure 5.

Instead of providing impedance goals, designers can optionally specify load-pull results directly from within Microwave Office software. The user simply needs to stipulate the goals, in this case 63% PAE and 51 dBm output power, instead of a specific impedance for each frequency point. In this instance, the automation built into the synthesizer tool works from performance goals rather than impedances, which is a much more intuitive approach. The synthesizer provides this capability for subbands in support of multi-band matching networks. Goals can be weighted differently, with all the available functionality that is built into the Microwave Office optimizer, such as sloped goals, being supported by the network synthesizer as well.

Additional goals that are not load-pull based can also be added. Figure 6 shows the overlap load-pull contours versus frequency and the initial synthesized matching network which follows the frequency trajectory of the contours over the desired bandwidth. User-specified target goals can be added to address harmonic terminations to improve linearity and efficiency. Extending the frequency range of the analysis shows that the synthesizer has generated a matching network to provide the desired impedance at the targeted fundamental frequencies as well as the second and third harmonic frequencies.

Post-Synthesis Review

At the end of the synthesizer run, a user-defined number of candidate networks are generated. This provides the designer with an easy and quick method to compare performance results for each network along with a pictogram of the generated layout to provide a visual aid to the designer, as shown in Figure 7.

Conclusion

NI AWR software provides network synthesis technology to accelerate design starts and explore design options using automated generation of impedance-matching circuits. The synthesis tool generates candidate networks based on user-defined goals, suggested element types to be utilized in the topology search, element constraints/limits, and more. The search engine explores possible topologies by expanding the solution up to the maximum number of sections as defined by the user. To learn more about the NI AWR Design Environment network synthesis wizard and other innovative features within the software, visit awrcorp.com/whats-new. ◄