Evaluation of Package Properties for RF BJTs

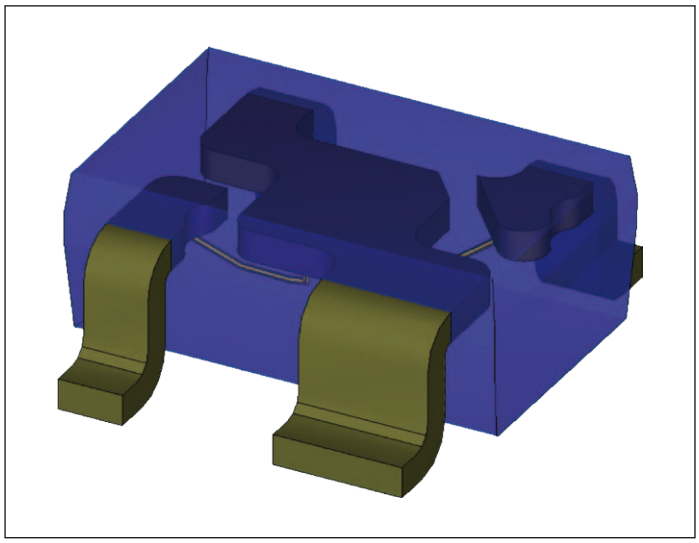

Figure 1: SOT343 package with BFP640 transistor IC from Infineon Technology

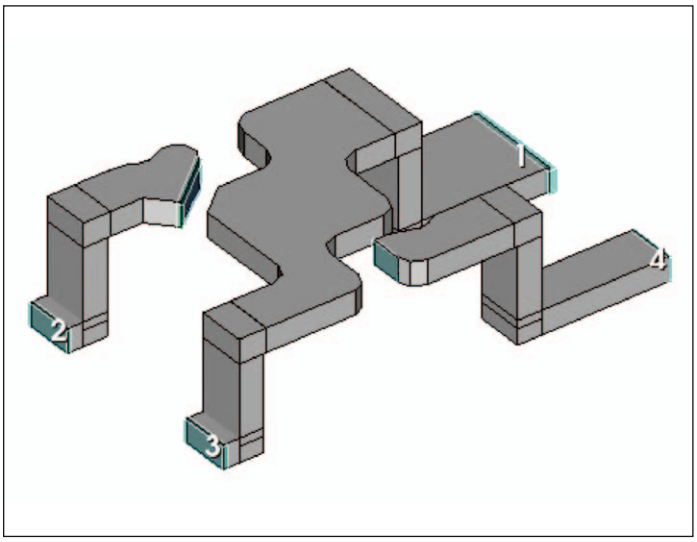

Figure 2: The SOT343 package partitions

This application note demonstrates the extraction procedure for the passive part of a SPICE model for the package and wire bonds of an Infineon Technology SOT343 bipolar junction transistor (BJT) up to 10 GHz and compares the model against measurements.

EDA simulation software streamlines the development of digital and analog circuits from definition of concept and estimation of required hardware and software characteristics to the design of system components like printed circuit boards (PCBs), chips, and packages. In particular, simulation technology for high-frequency (HF) and high-speed electronics enables designers to characterize parasitic effects at a wide range of frequencies and accurately predict performance. High-quality models are required and the better the model, the more likely that the functionality of the end product will correlate with simulated performance.

What Level of Preciseness?

A SPICE model is one possible schematic presentation, which is done using a text file. Components in the file show the modeled equivalent schematic of a device. A very important question in the creation of a model is at what level of preciseness should the model be extracted. Compared to digital, HF analog systems are less wideband, as the signal is very often concentrated close to the carrier frequency. In the case of a digital system, the digital signal is presented with wide spectra and the model should be characterized at a wide frequency range.

In an analog system, often the designer does not know what the working frequency of an analog component will be and must characterize it in a wide frequency range to cover all possible applications. It is also important to have correct DC modeling in order to have the correct biasing for nonlinear devices at the required frequency range if the device will need to go from the frequency domain to the time domain.

Another model parameter is impedance range, as the signal shape will be different depending on the impedance of the load ports. In practice, this means the impedances on the integrated circuit (IC) pins that are used in the design, so the model should provide correct work in the required impedance range.

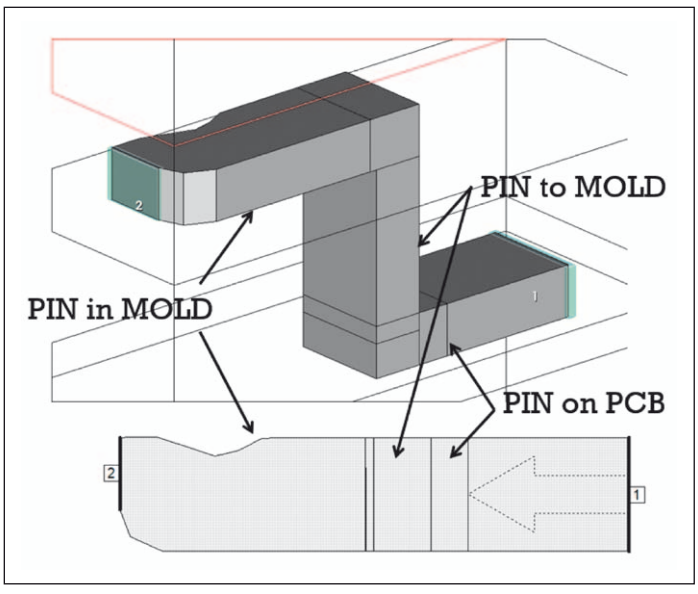

Figure 3: Three main parts of the pin

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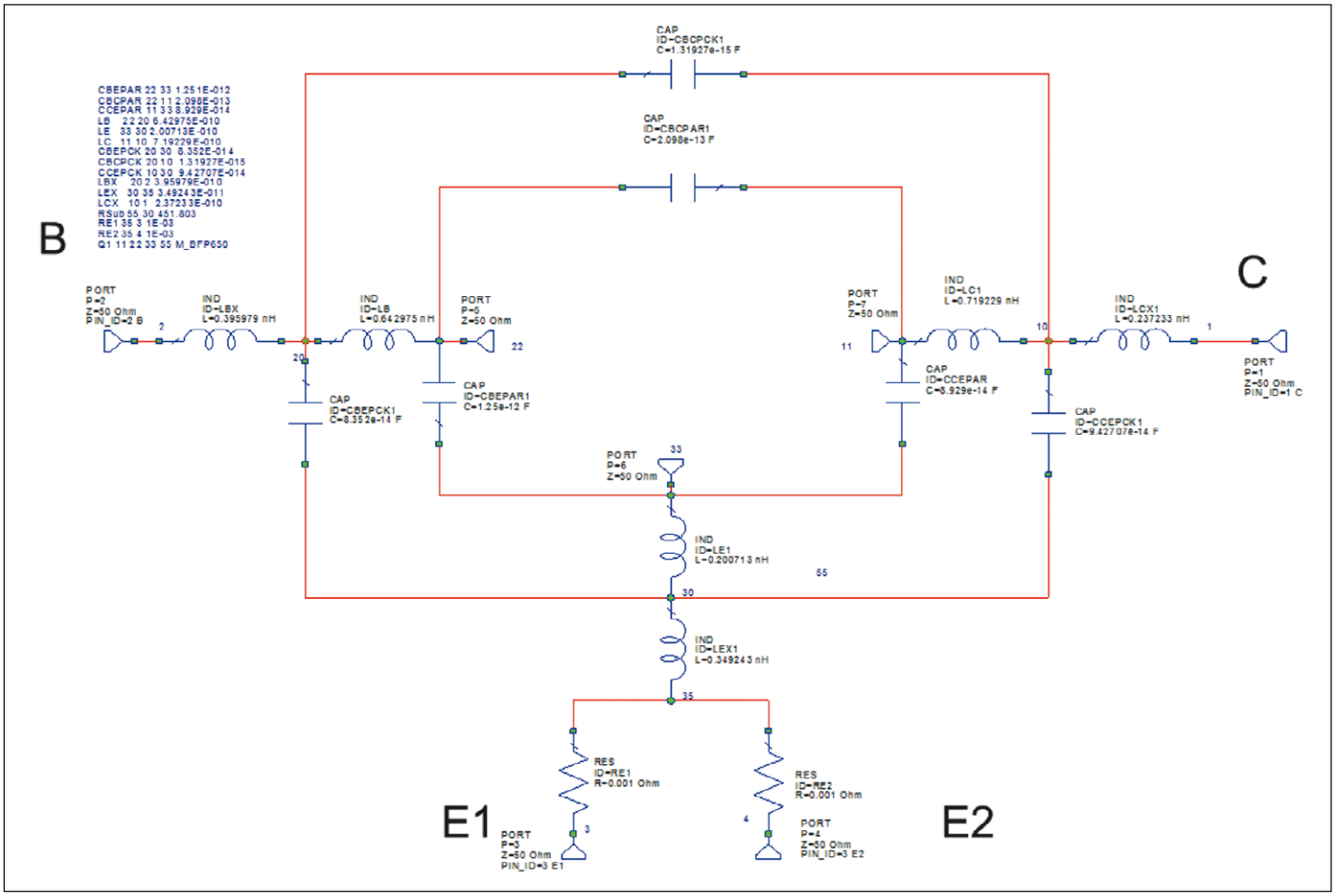

Figure 4: Example of a high-quality model

Extraction Procedure for BJT

The SOT343 package is used in many HF devices and its parasitics need to be considered in the performance of a semiconductor chip. Packages are soldered onto PCBs and distribution of current on the board's leads and bond wires adds inductive impedance and magnetic couplings.

Capacitance between leads and to the ground and other metal parts produces couplings between all these parts and must be included in the models.

The package was measured in different connection models on a test fixture and parts of the package were modeled with NI AWR Design Environment, specifically Analyst™ 3D electromagnetic (EM) simulator.

The package parts were then converted to lumped elements and a complete SPICE schematic was created, which was compared with measurement values.

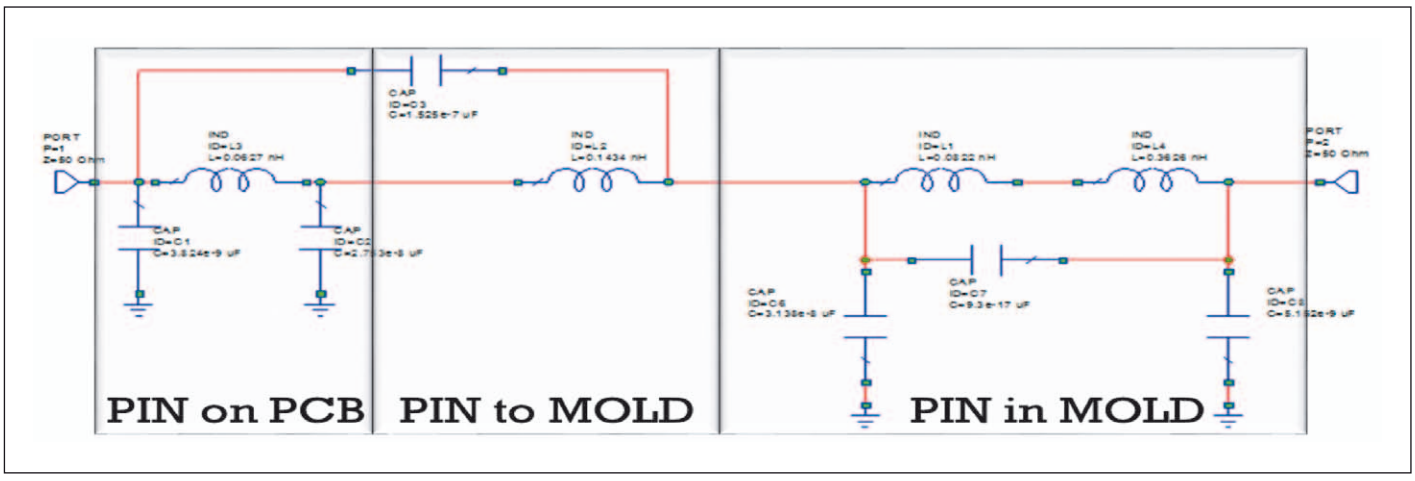

Figure 5: Example of the equivalent schematic of each part of the pin

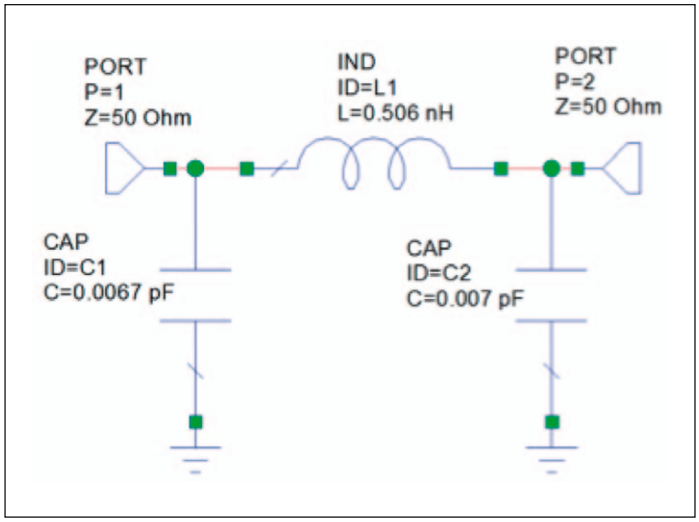

Figure 6: Example of the equivalent schematic of the bond wires

The electromagnetic compatibility (EMC) and signal integrity were analyzed in the time domain, where a series of bits were transmitted through the system. The binarity of the system provides robustness, but issues in the schematic design with the impedance of the IP pins, phase shifts, reflections, and cross-talks caused distortion of signal quality and failure to receive the correct bits. The bit error ratio (BER) indicated that there were significant problems in the design. Figure 1 shows the 3D layout in Analyst of the Infineon BJT package.

On a circuit level, the eye window for the signal is usually defined, the estimate of which allows distortion of the signal in all possible bit sequences. All these effects require high-quality models for simulation of modern cutting-edge systems to control them. Nonlinear components are included in addition to linear parasitic nonlinear effects. There are such formats as SPICE, IBIS, Touchstone port parameters, and more, which model the linear and nonlinear components and enable the design of analog, digital, or mixed-signal systems.

The SPICE model is a very popular simulation model that uses text files to present the equivalent schematic of the device with parasitic effects. It usually presents the physical structure of the device, which gives very good simulation quality, but opens the internal structure of device. The quality of modeling, as well as the design quality and speed, influence the economic aspects of the design. High-quality models reduce design time, as well as design and prototyping costs, because they require less redesign and prototype iterations, enabling earlier time to market and higher market share for electronic products. This is particularly important for next-generation technologies such as internet of things (IoT) and 5G communication systems, as systems with such complexity, density, and frequency range cannot be properly designed without precise modeling.

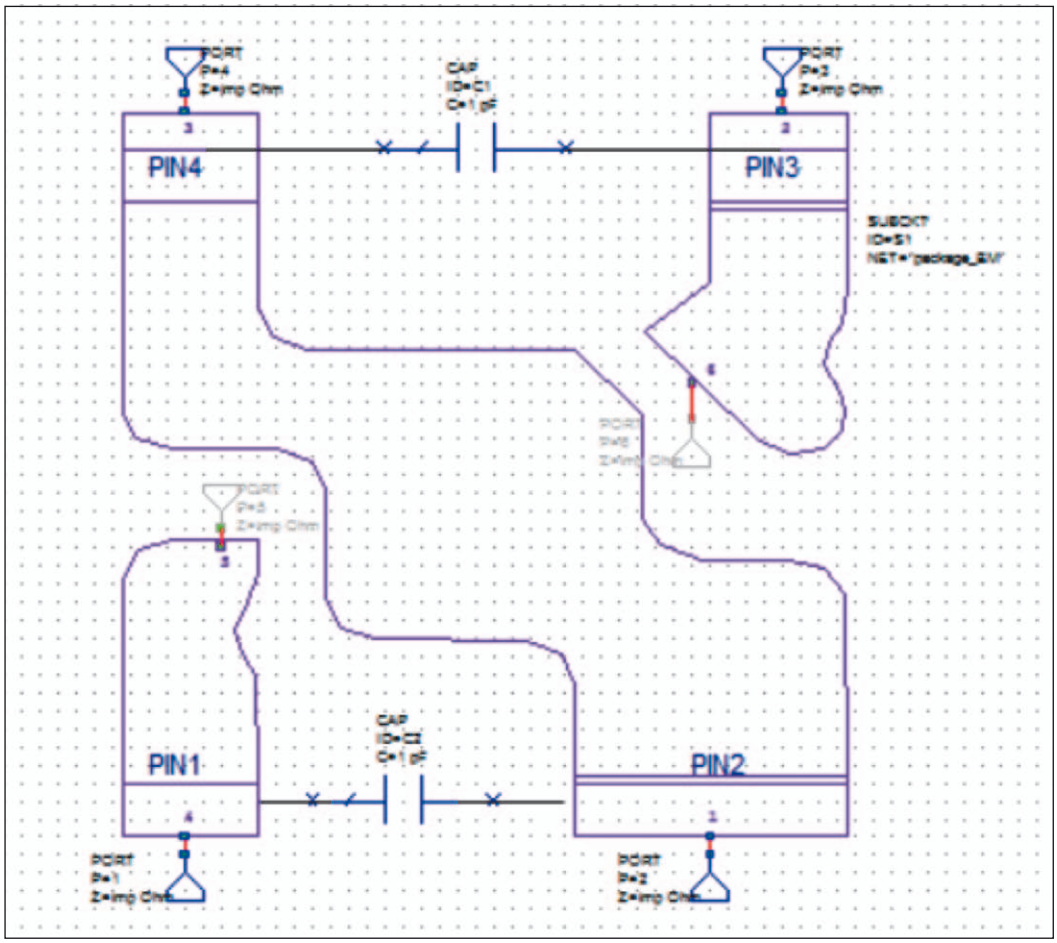

Figure 7: 1.5 W amplifier gain, output power, and efficiency after optimization for 12 V operation

Measurement Equipment and Settings

SPICE model development starts with an adequate EM model. The EM model should correspond to the real device, therefore the geometry and electric properties of the materials, as well as port settings of model, should correspond to the real-world material and user case. Comparison of the EM model simulation with measurements lets designers verify how close the EM model is to the real device. The calibration of measurement setup and consideration of the parasitic effects is another task required for correct comparison. When the EM simulation is close to the measurements, it can be used for EM extraction. A good way to compare the EM model with the real device is to compare the S-parameters obtained during EM simulation and measurements.

SPICE Extraction

SPICE format is one of the most commonly-used simulation models for EDA software tools. It can model linear and nonlinear circuits and include parasitic effects of the components. Including the main parasitic effects in the SPICE netlist makes possible correct wideband behavior of the model. S-parameters are

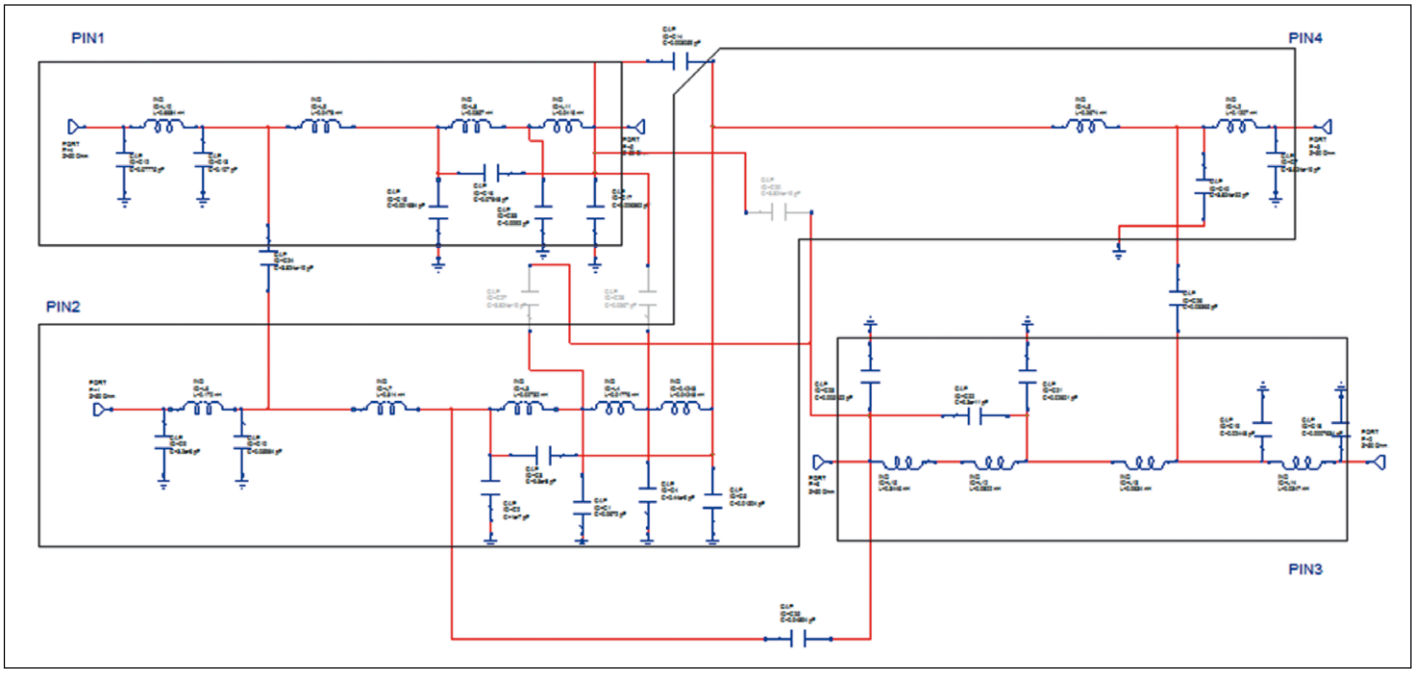

Figure 8: Schematic of the entire model

also often used for simulation of high-frequency devices, but this approach provides linear behavior only on the device pins, does not include the inner structure of the device (black-box model), and is not supported in many simulators, unlike SPICE. Usually S-parameters are the result of a measurements with certain temperature, calibration, and more. They have many advantages, but SPICE is more flexible and includes more information. SPICE can present an equivalent schematic in an EDA tool or in text format.

The review of existing SPICE models for packages shows that many electrical effects are not included in models. This reduces their precision and doesn't provide good correlation with measurement versus frequency. This can be seen after a comparison of measurement and simulation of these models. As a result, simulation results can't predict measurements of modeled devices.

Such differences can have a negative impact on the development of RF devices. For instance, a bad SPICE model will provide a wrong impedance calculation and the matching circuit will be calculated for the wrong impedance. This will cause the measured device to perform poorly. Only high-quality models can do this correctly and deliver an accurate prediction of circuit performance. Figure 4 shows an example of such a model.

Often models are done only for small frequency bands. For this, using S-parameters is sufficient, as they will be closer to the measurement.

In the next section a SPICE model extraction procedure is described. NI AWR Design Environment, specifically Microwave Office circuit simulation software, was used for extraction

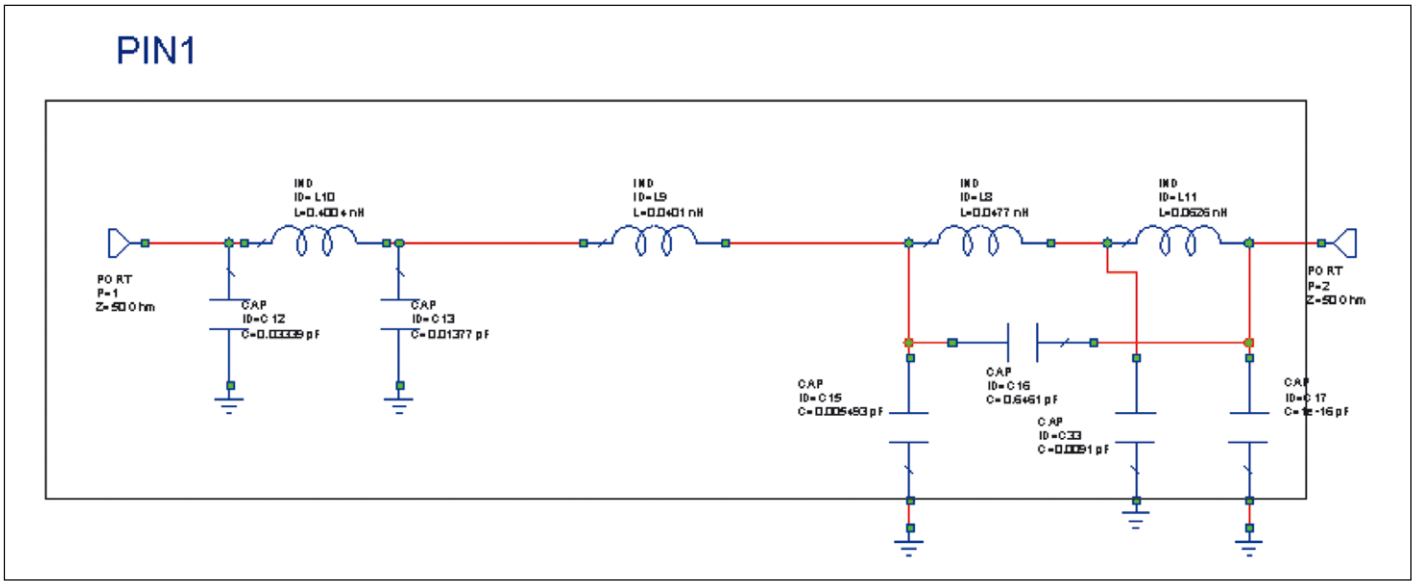

Figure 9: Testing for Pin 1

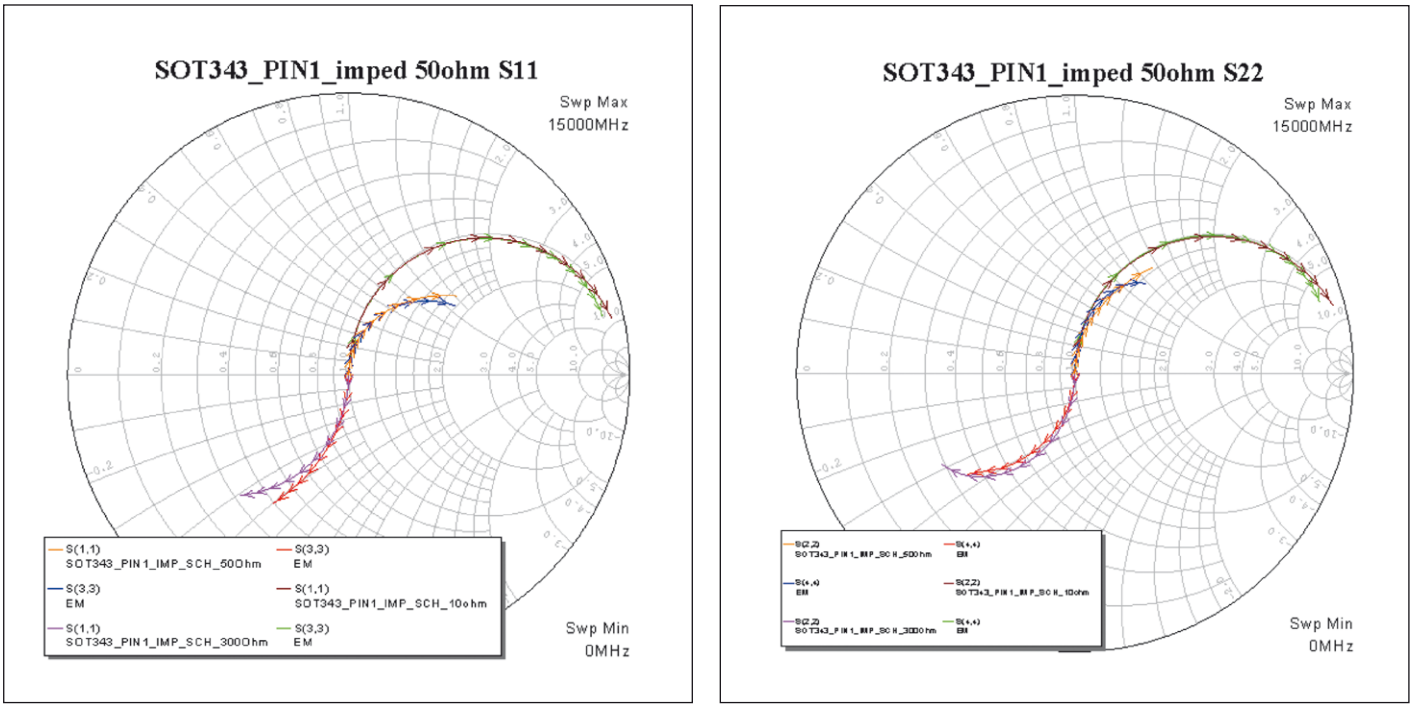

Figure 10: Simulation results for the SPICE model (left) and corresponding EM simulation (right)

because it provides a wide spectra of simulation tools required for successful extraction.

EM Simulation of Parts

The SPICE model must be based on the correct physical model, which is provided in Microwave Office. The development of the SPICE model was done using decomposition or partitioning of the package model on different parts. The SOT343 package contains the partitions shown in Figure 2:

Pin 1 – bond wire to chip
Pin 2 – bond wire to chip
Pin 3 – bond wire to chip
Pin 4 – bond wire to chip

These parts were simulated in separate EM simulations. Pins 1 and 3 were connected through the die pad and were included in the same EM model. Figure 3 shows the EM model for the pins. The pin contains three main parts: the part included in model compound, the transition between model part and outer lead part, and the lead connected later with the PCB. Each of these elements has its own parasitic characteristics. The sub-division enables the designer to discover dependencies that can't be seen in the whole simulation. Each part of the pin has its own equivalent schematic. An example of the equivalent model is shown in Figure 5. The same method is used to create the SPICE model of the bond wires. The equivalent schematic of the bond wires is shown in Figure 6. Each part can be simulated in decomposition.

Estimation of Interactions

Interactions between the simulated parts must be also included in the model. For instance, capacitance between the pins should be included, as shown in Figure 7.

Creation of Equivalent Circuit

Taking into account the parasitics of the package pins and die pad and their interactions, the entire model can now be created (Figure 8).

Validation of Model in Frequency and Impedance Range

Quality assurance of the equivalent circuit of the package is completed by testing each of the pins and also by testing the com-

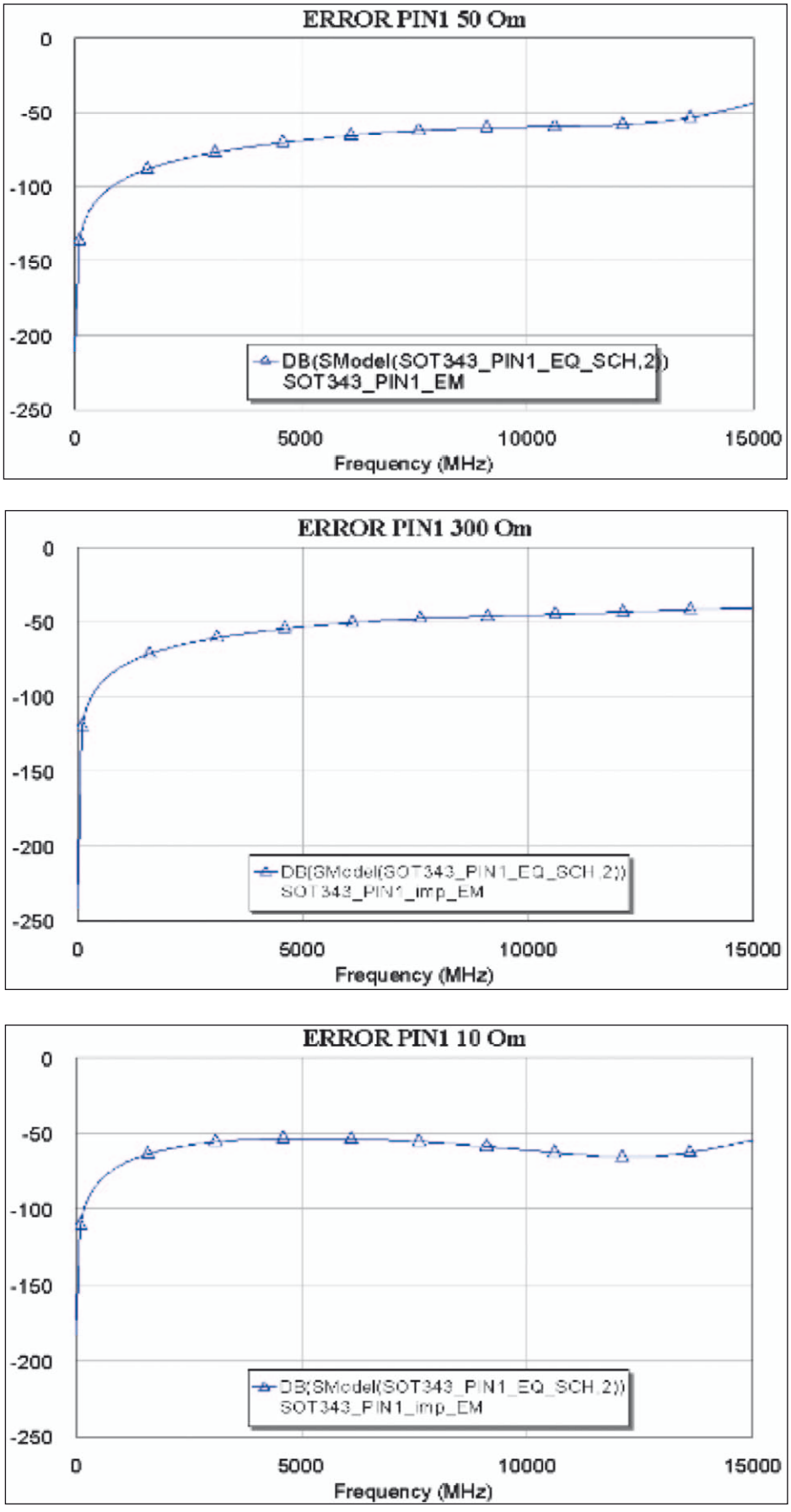

Figure 11: Simulation results for the EM and SPICE models at 50 Ohms, 300 Ohms, and 10 Ohms

plete model with different port impedances. Testing on this model was made on the 100 Ohm, 50 Ohm, and 10 Ohm port impedances. Testing for Pin 1 is shown in Figure 9. The differences between the SPICE model and the corresponding EM simulation are shown in the Smith charts in Figure 10.

The differences between the EM and SPICE models were numerically modeled and the results of the testing on Port 1 are shown in the graphs in Figure 11. It can be seen that the differences between the models did not exceed the -50 dB threshold. The same tests were done on Ports 2, 3, and 4.

Conclusion

Product development cycles are among the most critical aspects in the development of electronic devices, as they define cost, performance, and time to market. Fast development time and the possibility of fast tuning and design reuse have become important competitive factors. From a practical perspective, this means that the performance of devices predicted in simulation software must be very close to measured performance. A high correlation between calculated performance during design time and obtained performance strongly depends on the quality of simulation algorithms, as well as the quality of the component models.

This application note has described the investigation process and results of package performance for a BFP650 BJT NPN transistor package. The quality and accuracy of the simulation using NI AWR Design Environment for 3D EM simulation and parasitics extraction was verified with measured results. The quality of package model was improved and a new model was created.

Problems during the verification of semiconductor devices is the result of a combination of active and passive parts in the whole device. Because EM simulation can't predict performance of nonlinear parts, the precision depends on the quality of the nonlinear model and comparison of measurement and simulation is not possible. In this case, the correlation of EM simulators can improve predictability.

In this application note, the correlation between measurement and simulation was done using packages with different combinations of bond wires. Analyst enabled the designer to model the geometry of these devices and provided results close to measurement.

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