Addressing Efficiency and Linearity with a Single-Ended Class AB Power Amplifier with optimized Third-Harmonic Termination (part 1)

This application note describes the design of a single-ended PA using Class AB "sweet spots" and an optimized third-harmonic termination based on a design flow that encompassed analysis of the requirements and initial concepts to the simulation, fabrication, and measurement of the built prototype.

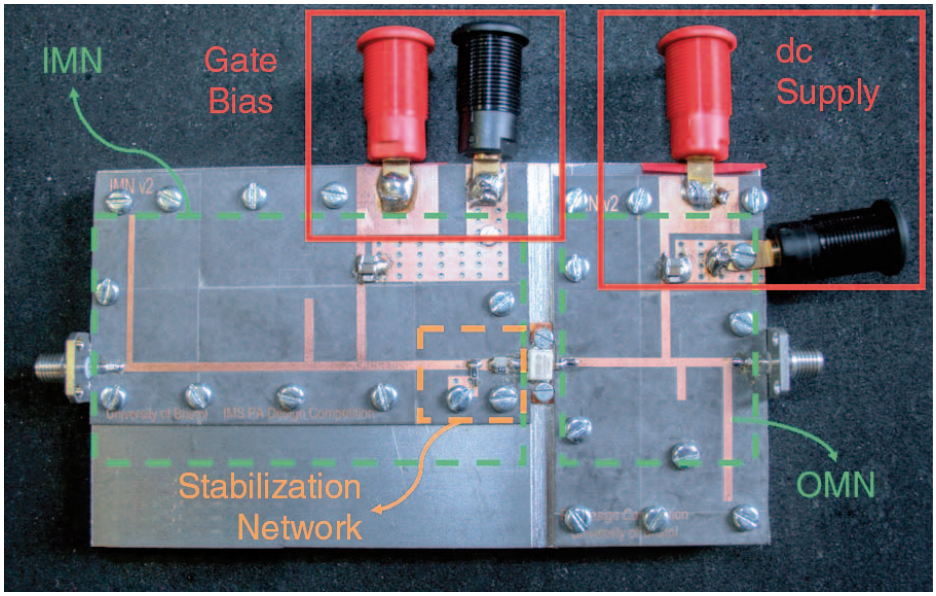

Figure 1: Annotated photograph of completed PA

The single-ended RF power amplifier (PA) is a standard design approach in the RF engineer's tool kit, but high efficiency and good linearity may only be achieved if the harmonic terminations and biasing conditions are carefully examined.

The design won first place at the 2016 International Microwave Symposium's High-Efficiency PA Student Design Competition.

Design Challenge

The main challenge of this design was to maximize the overall power-added efficiency (PAE) of the PA while amplifying a time-varying envelope signal, without compromising the linearity performance. The design specs required the achievement of the highest PAE as measured for a two-tone input signal while at the same time ensuring that the carrier-to-intermodulation ratio (measured third-order intermodulation distortion [IMD3] level) was lower than –30 dBc.

A figure of merit (FOM) was calculated from this measurement according to:

$$FOM = PAE \times (f_r)^{1/4} = \frac{P_{out} - P_{in}}{P_{DC}} \times (f_r)^{1/4}$$

where the PAE is weighted by the operating frequency fr in gigahertz to compensate for the greater technical challenge in the higher-frequency design. P_{out}, P_{in}, and P_{DC} refer to the RF output power of the two tones of interest, the RF input, and DC power supplied, respectively.

The PA design operated at 3 GHz and used a packaged Wolfspeed [formerly Cree] gallium nitride (GaN) high-electron mobility transistor (HEMT). The prototype PA, shown in Figure 1, achieved a maximum continuous-wave (CW) output power of 36.2 dBm and a two-tone PAE of 44 percent at –30 dBc IMD3, while delivering 34.04 dBm of output power.

Problem Formulation

At the beginning of a design project, it is necessary to analyze the full range of specifications and survey prior designs that achieved similar results.

Specifications for the design were:

- Fewer than 24 dBm (250 mW) of input power to reach the point of saturation in the presence of a CW signal and produce an output power between 36 dBm (4 W) and 50 dBm (100 W) at saturation
- Fewer than 22 dBm (158 mW) per tone to reach the point of saturation in the presence of a two-equal-tone signal with 5-MHz tone spacing

Special Thanks to Paolo Enrico de Falco James Birchall and Laurence Smith for their Contribution to the application note National Instruments ni.com/awr

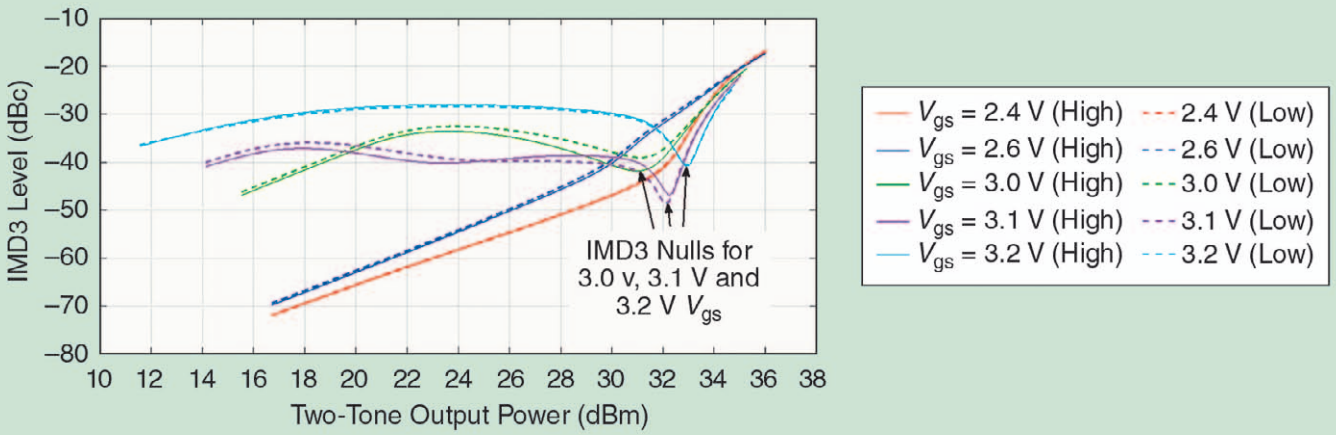

Figure 2: The simulated IMD3 versus output power, showing the varying profile and the nulls in IMD3 for different gate bias voltages

• Use a maximum of two DC power sources

• Operate in the 1–10 GHz frequency range

The main constraint placed on the design was the large-signal CW gain, which had to be above 12 dB at saturation to achieve the minimum output power of 36 dBm. For the operating frequency, values between 3 and 5 GHz were considered because, due to the frequency dependence of the FOM in Equation 1, a higher value would result in only a small FOM improvement. GaN transistors were chosen for their performance at multiple gigahertz frequencies and because by operating at the low end of the 36–50 dBm range, their efficiency could be further enhanced.

A two-tone signal with 5-MHz frequency spacing was used to evaluate the design. Closely spaced two-tone signals have a variable time-domain envelope with a 3-dB peak-to-average power ratio, so PAE over a 3-dB backoff range needed to be improved to avoid degrading the average efficiency. Finally, it should be noted that the PAE was measured at -30 dBc IMD3 rather than at saturation.

For conventional amplifiers, the PAE was seen to increase monotonically until heavy compression occurred, so, to maximize the measured PAE, it was helpful to maintain a linear power transfer characteristic until saturation. A trade off between linearity

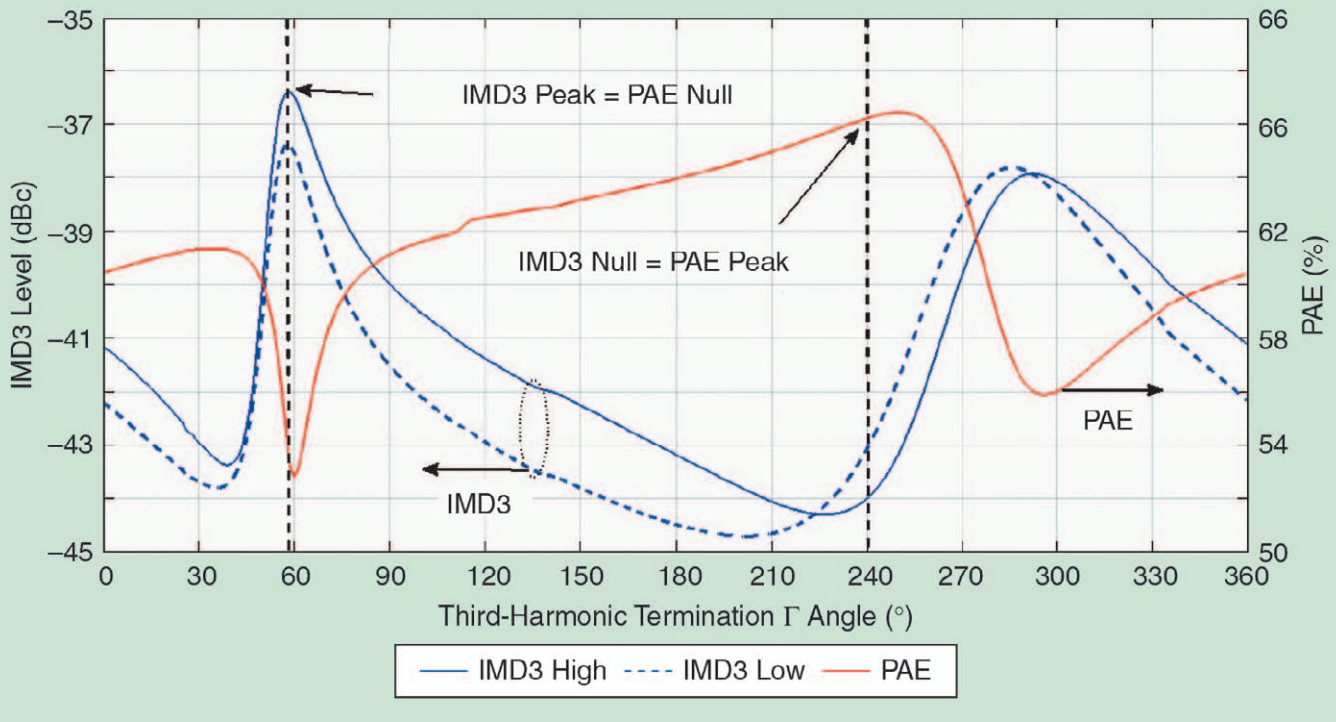

Figure 3: The simulated IMD3 and PAE versus the third-harmonic reflection coefficient angle, illustrating the matching peaks and nulls of the two profiles

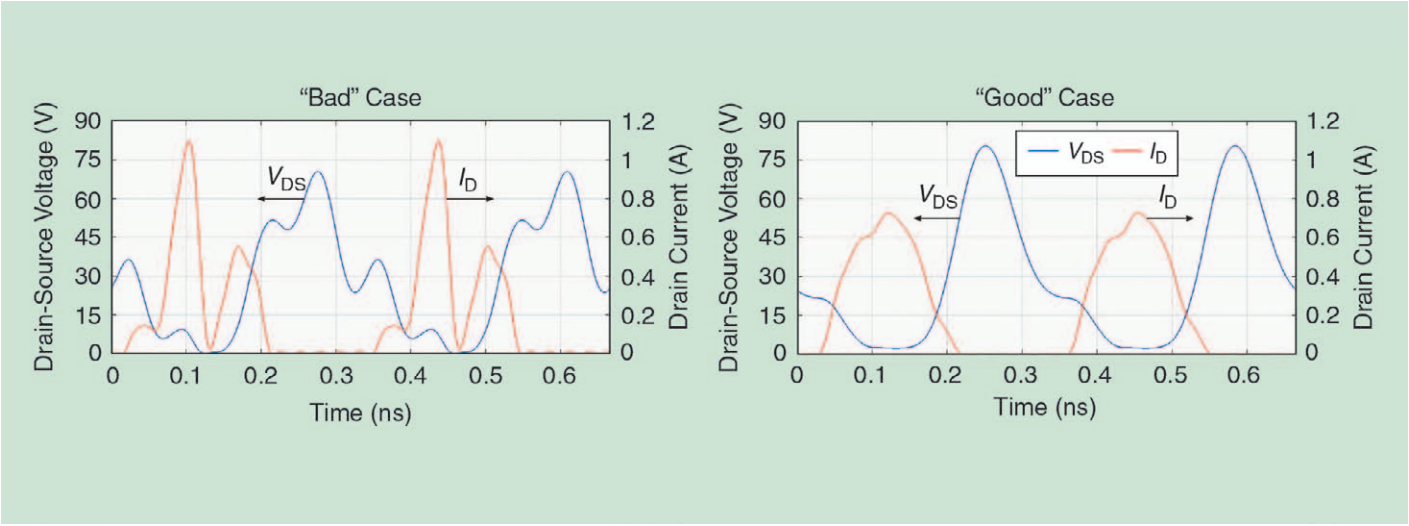

Figure 4: The intrinsic drain-source voltage and drain current waveforms for a) "bad" and b) "good" third-harmonic impedance termination

and efficiency was, therefore, inevitable, and a good balance was crucial to achieve the desired FOM.

Design Solution

The linear DPA architecture has been shown in other designs to adapt well to the design requirements providing remarkable results due to a number of features that complement the specifications. Broadly speaking, the active load pull of the main amplifier by the peaking amplifier ensures improved efficiency in the back off region. Through the appropriate choice of biasing - Class AB for the main and Class C for the peaking - the compressive and expansive nature of the transfer characteristics of the two branches can be exploited to compensate for one another, thereby suppressing IMD3 and enabling linear operation up until saturation.

Improving on previous design performance was thus no easy task. One option considered was to increase the degree of load modulation compared to the previous linear DPAs, which could boost the efficiency at back off. However, this would only be obtained if the linearity of the main amplifier's transfer characteristic could also be improved, allowing for the peaking stage to turn on when the main amplifier has maximum (or close to maximum) voltage swing. Ultimately, the designer decided to focus on extending the linearity of a single-ended PA through exploiting specific operating condition values for Class AB gate bias values that are found to improve the linearity of the PA's power transfer characteristic, while also tuning the third harmonic termination.

Despite having drawbacks in terms of performance when compared to a linear DPA solution, a single stage design has several practical advantages, including a single active device, less extensive biasing and matching circuitry, simplicity for implementing and iterating, and low cost and form factor.

Moreover, a strong understanding and characterization of a linear, single-ended Class AB amplifier provides a good foundation for the design of the main amplifier stage in a DPA or other load modulation-based architectures.

In Class AB PAs, the nonlinearities introduced by the output current waveform's truncation (which is, itself, a function of input drive level and bias) can compensate for the weak nonlinearities introduced by the transistor to produce favorable linearity performance at a given drive level. Specifically, for deep Class AB conduction angles, the current waveform truncation causes a compression of its fundamental frequency component with increasing drive level, which can compensate for the expansive characteristic exhibited by real-world transistors in the turn-on region. For two-tone signals, this translates into local minima, or "nulls," in the IMD3 profile at certain points in the amplifier's response, as shown in Figure 2. (In the graphs in the figures that follow, "high" and "low" refer to the IMD3 measured for the intermodulated components above and below the two carrier tones, respectively.)

To further improve efficiency and increase the linear dynamic range of the amplifier, the appropriate impedance terminations must also be considered. Prior work has mostly addressed the impact of the second-harmonic impedance termination on linearity. However, little investigation has been done in considering the effect of third-harmonic termination on linearity, which is particularly significant in Class AB PAs.

Figure 3 shows the result of a harmonic balance (HB) CW simulation sweeping the third-harmonic impedance at a constant input drive level for a Class AB PA, with fundamental and second-harmonic impedances optimized for PAE. As the figure indicates, the effect on PAE and IMD3 is notable, with the null in IMD3 corresponding to a peak in PAE and vice versa.

This is due to an appropriate third-harmonic short, which promotes a correct shaping of the voltage waveform and reduces the overlap in current and voltage at the current generator (CG) plane of the transistor. This is further shown in Figure 4, which illustrates the intrinsic voltage and current waveforms for different cases of third-harmonic termination, which will be further explained in the following section.

The designer chose NI AWR software, specifically Microwave Office circuit design software for all circuit simulations and focused on finding accurate models for the devices and lumped elements used. Following an extensive survey of packaged GaN HEMT devices, the Cree CGH40006P was selected based on its highly accurate and verified large-signal model and its power and gain-frequency performance. The microstrip circuitry was modeled using AXIEM 3D planar electromagnetic (EM) simulator and Murata high-precision ceramic capacitors were chosen for their accurate parasitic model. ◄