High efficient heat dissipation on printed circuit boards

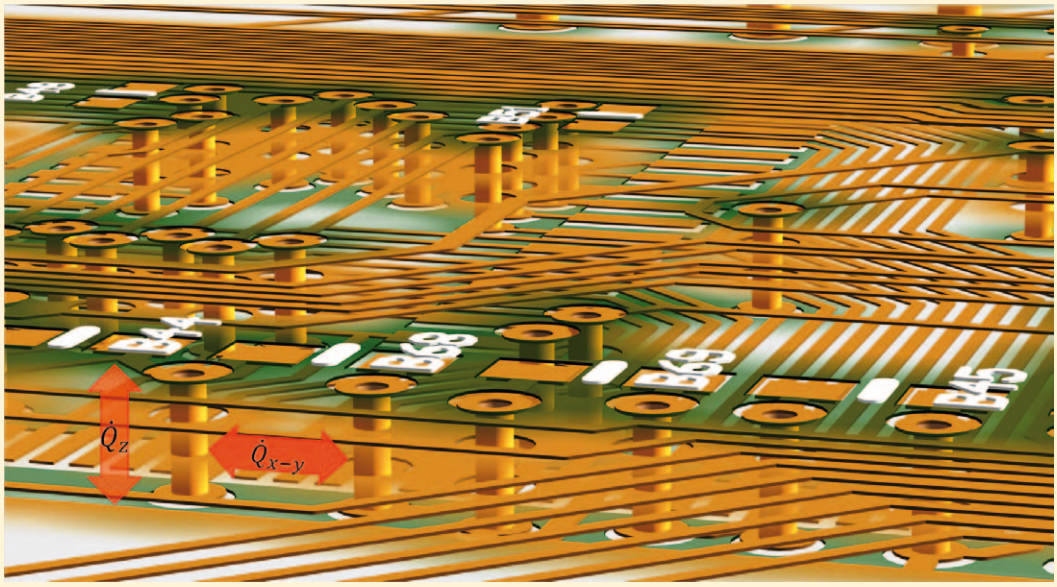

Figure 1: Heat flux in a PCB

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Abstract

This paper describes various techniques for dissipating heat from heat generating electrical components on printed circuit boards (PCBs). Small copper coins that are matching the shape of the electrical components are located underneath the component and are integrated into the PCB construction. The heat from the component will be dissipated by the copper coin to a heat sink or cold plate. The thermal conductivity of such kind of copper coin is about 10 times higher than usually achieved with so called thermal via arrays. Several different methods of integrating copper coins into the construction of PCBs have been developed and will be discussed.

New developments such as the "Chip-on-Coin" technique are providing solutions for highly miniaturised electronic circuits and micropackaging. The integration of copper coins into PCBs is suitable for all common substrates including RF and microwave substrates as well as for conventional PCB substrates. (Key words: PCB, heat dissipation, thermal via, copper coin, press-fit, bare die attach.)

Introduction

Controlling the heat loss of electronic and microelectronic systems is a more and more challenging task as miniaturisation is increasing, and the growth in functionality is driving the components to their limits, which means that they are generating more heat loss. Printed circuit boards are the carrier of the components and are therefore also highly involved in the matter of controlling the heat.

The PCB by its nature is not a good thermal conductor. It is made of substrate materials that are insulating electrical interconnections between components. The thermal conductivity of a typical substrate material is about $\lambda \sim 0.2$ W/mK. However, copper, the material of the conductive traces of a PCB, has a high thermal conductivity of $\lambda \sim 390$ W/mK. Depending on the copper distribution the heat flux in a printed circuit board is normally better in the x-y plane compared to the heat flux in the z-axis (Figure 1).

A power or ground plane has a bigger influence on the heat flux. The heat flux and direction is mainly dominated by the thermal conductivity of the materials and the ΔT in a given area.

The conductive traces of a PCB in practise cannot be used as a good and efficient thermal conductor. Their cross sectional area is simply much too low.

Many microelectronic components are designed with a predetermined thermal pathway inside their packages (Figure 2).

The thermal loss of a plastic ball grid array (P-BGA) for example is dissipated via the base of the

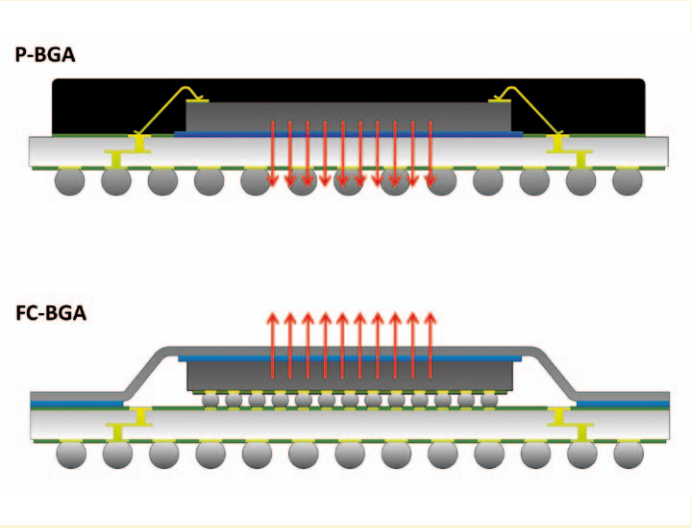

Figure 2: Thermal pathway inside component packages

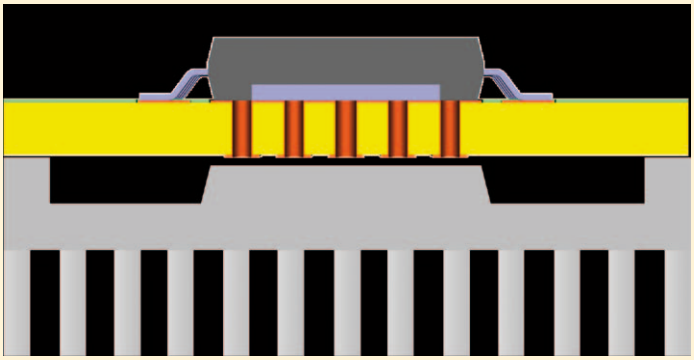

Figure 3: Thermal vias in a PCB

package whereas in a flip chip ball grid array (FC-BGA) the thermal loss is guided to the top surface of the package.

The principle that the thermal loss of a component is transferred to the base of the package provides the ability to integrate a path for heat dissipation into the physical construction of a printed circuit board.

A very common approach is to place an arrangement of vias as so called thermal vias in the PCB underneath the component (Figure 3).

The base of the component is connected to the thermal vias on the top side of the PCB. The heat flux is transferred through these vias down to the bottom side of the PCB and then coupled into the heat sink or a cooling plate. For heat spreading the thermal vias are sometimes connected to power or ground planes of the PCB.

This principle is widely used at nearly any extra charges because PCBs consists of lots of lots of vias anyway. The question is how efficient are thermal vias? They may work fine for many applications but the effective thermal conductivity of thermal vias is low due to the small amount of conductive materials that are involved. The heat flux flows mainly only through the very small cross sectional area of the copper plating at the hole wall of the vias. The centre of the vias remains usually open and unfilled, and the surrounding material is the substrate material of the PCB which is a good insulator.

Local Heat Dissipation By Copper Coins

To create a much more efficient path for heat dissipation the idea is to replace the arrangement of thermal vias by some piece of solid metal to increase substantially the amount of conductive material of thermal via arrays.

The goal was to find methods and techniques that are compatible to the constructions and the manufacturing processes of printed circuit boards and that are suitable for any assembly processes. The material of choice is copper because of its high thermal conductivity and its excellent compatibility to PCB production processes.

Several methods have been developed:

- press-fitted copper coins,
- adhesive bonded copper coins,
- embedded copper coins.

All these methods are using solid pieces of copper that are integrated into the mechanical construction of the printed circuit board during its origin production process.

Press-fitted copper coins

The insertion of copper coins in printed circuit boards by means of the press-fit method is a very cost effective technique that is practised e. g. on PCBs for engine controls in the automotive industry or for power amplifier in base stations of wireless networks.

Copper coins are pressed in an intermediate production step into

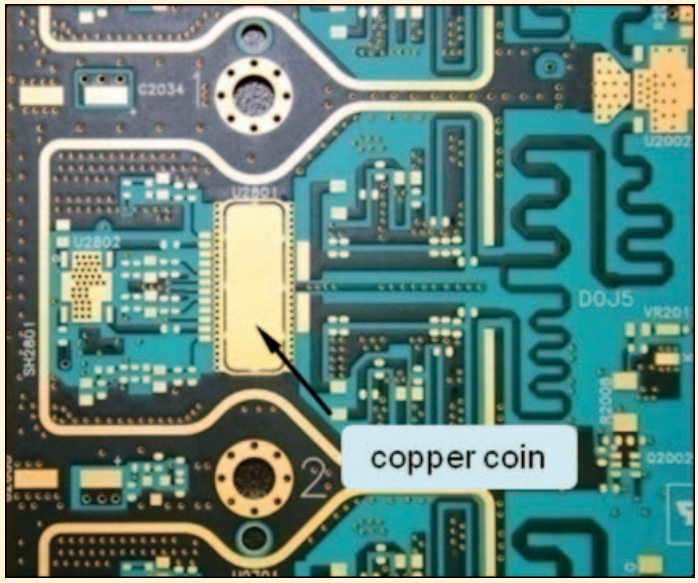

Figure 4: PCB with press-fitted copper coin

appropriate openings of printed circuit boards. The openings can be plated or non-plated. After the coin insertion the normal production process flow continues. Figure 4 shows a segment of a printed circuit board with press-fitted copper coins.

The copper coin is designed with a number of specific ribs along the outer peripheral surface helping to control how strong the coin is fastened in the cut-out of the printed circuit board. The ribs are also maintaining the electrical connection between copper coin and PCB, e. g. the grounding.

Adhesive bonded copper coins

Another method is to attach the copper coins onto the PCB when the normal fabrication process has been finished. The copper coins are bonded to the PCB in defined locations by using thermally and electrically conductive film adhesives (Figure 5).

The copper coin in Figure 5 has a flange the spreads the heat and enables a better thermal connection to a heat sink or cold plate by enlargement of the effective surface area. It also carries the adhesive preform (grey colour).

The bond strength of the bonded copper coins depends on the adhesive used, the type of surfaces, and also on the size and geometry of the bonded area.

Depending on the selected adhesive the coin can be thermally and electrically connected to the PCB or insulated or only

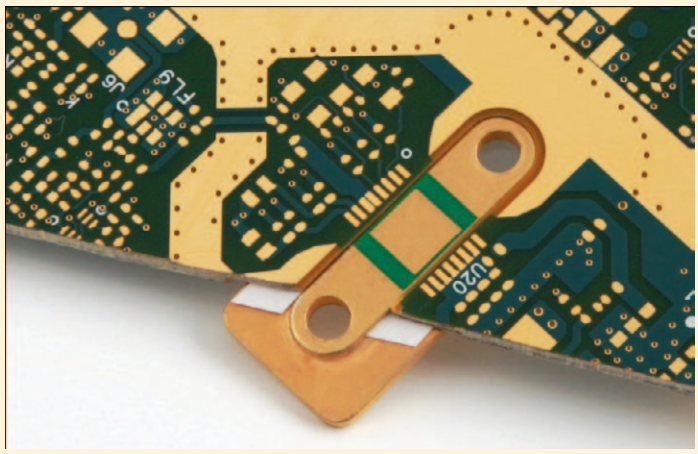

Figure 5: PCB with adhesive bonded copper coin

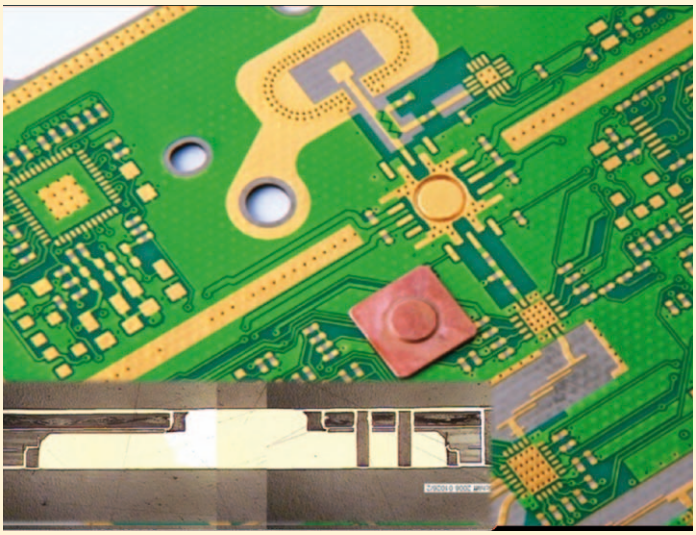

Figure 6: PCB with embedded copper coin

thermally or only electrically connected.

Embedded copper coins

If the copper coin is integrated into the construction of the printed circuit board at the same time and with the same process when all other layers of the PCB are laminated together then this method is called embedded copper coin. Window cuts are prepared into the cores and prepregs of a PCB stack and when the stack-up construction is assembled prior lamination the copper coins are placed into the window cuts. The embedded copper coins can be electrically connected to the PCB by plated through holes and galvanic copper deposition on the surface layers (Figure 6).

The embedded copper coin is fully integrated in the layer construction and lies flush in plane on both sides of the printed circuit board.

The press-fitting of copper coins is the most cost efficient technique of the three described methods in this paper. However, the press-fitting technique is limited to a maximal size of approx. 40 mm x 40 mm to avoid overstressing the PCB with a too high mechanical load during the press-fitting process. Therefore, the two other methods can be seen as back-up solutions for the case that press-fitted copper coins are not the best suitable technique for a specific application.

Further Designs And Developments

Copper coins with cavities

Some high power transistors are housed in packages with metal flanges for heat spreading and dissipation. They are normally soldered or bolt down on heat sinks or cold plates. The copper coin technology provides a solution to assemble such devices directly onto a printed circuit board (Figure 7).

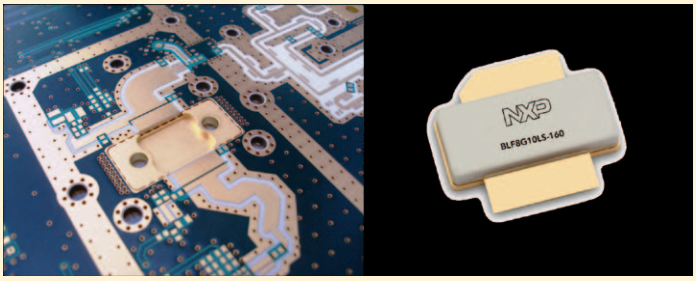

Figure 7: Press-fitted coin with cavity

Thermal via array, 5 x 5 mm, via diameter = 0.5 mm, PCB: 1.5 mm thick FR-4	λ W / mK	R_{th} K/W
Vias plated with 25 microns thick Cu	14.5	4.1
Vias plated with 27 microns thick Cu	15.6	3.8
Vias plated with 30 microns thick Cu	17.2	3.5
Vias (25 microns thick Cu) filled with conductive Silver paste	15.4	3.9
Vias (25 microns thick Cu) filled with solder	25.2	2.3
Vias filled with copper	75.9	0.8
for comparison: 1 copper coin, Ø 4 mm	194	0.3

Table 1: Effect of via filling

The copper coin of Figure 7 includes a cavity in which the flange of the power transistor will be placed for assembly. The design of the cavity matches perfectly to the shape and design of the flange. The depth of the cavity is designed in such a way that the flange is fully captured while the leads of the power transistor are aligned straight over the solder pads of the PCB for best performances. This method provides the opportunity to assemble such power devices in an automated process directly onto the PCB without the need of some manual operation. Cavities can be designed into any of the copper coin methods described in this paper.

Chip-on-Coin

The latest development on copper coin technology is addressed to bare die attachment. The well known chip-on-board technology (COB) is used to reduce physical space (miniaturisation) and therefore improves signal performance (signal integrity) and speed. But it also eliminates the package of the die which could be used for a new approach for heat dissipation: the Chip-on-Coin technique.

The bare die is attached directly on a copper coin of the printed circuit board. The elimination of the housing of the die provides an advantage for the heat dissipation compared to conventional housed components because some thermal boundaries are removed from the thermal pathway. The lower number of thermal interfaces in the thermal pathway leads to a reduced overall thermal resistance and to a much higher efficiency in the heat dissipation of the chip. Compared to components in packages the junction temperature falls. The mismatch of the thermal expansion between the copper coin and the substrate

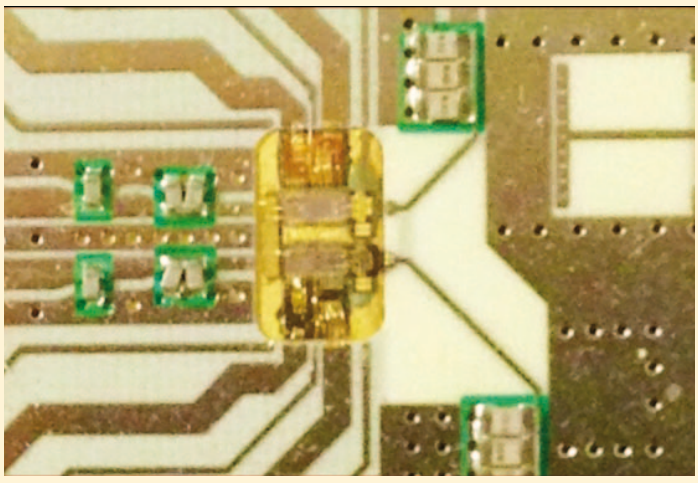

Figure 8: Chip-on-Coin technique

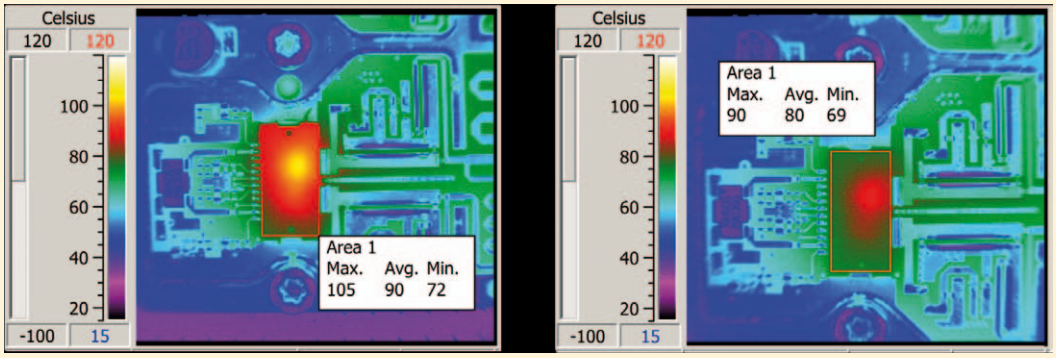

Figure 9: left: thermal vias, right: copper coin

material of bare dies can be compensated by replacing copper with some material compositions that are better suited for direct die attachment such as Tungsten-Copper or Molybdenum-Copper. An example of the Chip-on-Coin technique is shown in Figure 8. An arrangement of bare dies is attached on a coin that is integrated into the PCB construction. The dies are connected with the PCB by wire bonding.

Thermal Vias Versus Copper Coins

The better efficiency of copper coins compared to thermal via arrays can be analysed with thermographic images (Figure 9).

Figure 9 shows two thermographic images of the power transistor stage shown in Figure 4. In the left hand image the power transistor is mounted onto an array of thermal vias. The maximal temperature of the component was measured to 105 °C. The power transistor in the right hand image is placed over a copper coin that is press-fitted into the PCB. The maximal temperature for this case is only 90 °C.

As the copper coin has a higher thermal conductivity than an array of thermal vias of the same size the temperature of the power transistor is reduced by 15 °C in this example. This is a significant reduction of the temperature of the component that could increase the life time and reliability of the component and the whole system.

Some calculations

To illustrate the performance of copper coins versus thermal via arrays we can calculate the thermal conductivity and the thermal resistance.

The effective thermal conductivity $\lambda_{eff\,1}$ and the thermal resistance $R_{th\,1}$ of a thermal via array can be calculated with the following equations:

$$\lambda_{eff\,1} = \frac{1}{A}\left(\lambda_{hole} \cdot A_{hole} + \lambda_{via} \cdot A_{via} + \lambda_{mat} \cdot A_{mat}\right)$$

$$R_{th1} = \frac{d}{\lambda_{eff\,1} \cdot A}$$

and for a thermal pad with copper coin $\lambda_{eff\,2}$ and $R_{th\,2}$ in a similar way:

$$\lambda_{eff\,2} = \frac{1}{A}\left(\lambda_{coin} \cdot A_{coin} + \lambda_{mat} \cdot A_{mat}\right)$$

$$R_{th2} = \frac{d}{\lambda_{eff\,2} \cdot A}$$

Where

$\boldsymbol{\lambda_{eff\,k}}$ is the effective thermal conductivity,

$\mathbf{R_{th\,k}}$ is the thermal resistance,

A is the surface area of the thermal array or the thermal pad,

$\boldsymbol{\lambda_i}$ is the thermal conductivity of the centre of the via (hole), the copper of the vias (via), the substrate material (mat), and the copper coin (coin),

$\mathbf{A_i}$ is the surface area of all centres of the vias, of all copper in the vias, of the substrate material in the array or pad, and the coin,

d is the thickness of the PCB.

As an example we calculate the thermal conductivity and the thermal resistance of a thermal via array and a thermal pad with copper coin as shown in Figure 10. Both fields are same in size, 5 x 5 mm. The thermal via array consists of 25 vias with a diameter of 0.5 mm and a copper plating thickness of 25 microns in the vias. The copper coin has a diameter of 4 mm.

The thermal conductivity of the thermal pad with the copper coin is $\lambda_{eff\,2}$ = 194 W/mK and for the thermal via array we get the result of $\lambda_{eff\,1}$ = 14.5 W/mK. Assuming a PCB thickness of 1.5 mm we get a thermal resistance for the thermal pad with copper coin of $R_{th\,2}$ = 0.31 K/W and for the thermal via array $R_{th\,1}$ = 4.14 K/W.

It can be seen that the thermal conductivity of the thermal pad with a copper coin compared to a thermal via array is more than 10 times higher, thus the thermal resistance of the copper coin is more than 10 times lower.

The effect of via filling

The example of the preceding section can be used to discuss the effect of filling the vias in the thermal via array (Table 1).

The centre of the vias can be filled to enhance the thermal conductivity by replacing the air with some material of better thermal conductivity. They can be filled with conductive Silver paste which increases the thermal conductivity only slightly. That small gain in thermal conductivity could also be achieved when a few microns of additional copper are plated into the vias.

A filling of the vias with some kind of solid metal such as solder or copper results in a much better thermal conductivity if a void-free filling can be achieved. However, via filling with electrolytic deposited copper in mass production is currently only feasible at a low aspect ratio (typ. 1:1), e. g. for microvias. In whatever way via filling is applied it will not reach the performance level of the copper coin method.

Reliability

For PCBs with copper coins it is necessary that the coins are integrated into the PCBs with a high level of mechanical precision to meet specific parameters and specifications such as flatness requirements for QFN components as an example. Also the press-fitting process shall not harm the surrounding area of the cut-out of the PCB when the coin is pressed in. Therefore, the process of attaching copper coins into the construction of the PCB has been carefully develo-

Test	Parameter
Lead-free reflow soldering (10 x)	J-STD-003A
Thermal shock	1000 cycles: - 55 °C to + 125 °C
Thermal stress	6 x 10 sec. on 288 °C solder float bath
Ageing (temperature storage)	1000 h at 125 °C
Electrochemical migration (humidity storage)	1000 h at 85 °C and 85 % r. h.
Delamination test	pre-cond. 72 h at 40 °C, 92 % r. H. solder stress 20 sec. at 288 °C
Push-out force	typ. > 500 N (dep. on coin design and size)

Table 2: Reliability tests

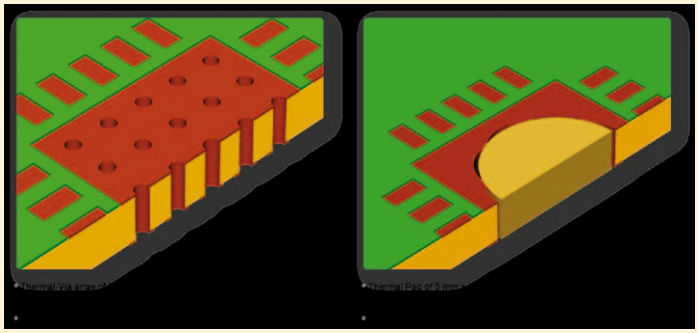

Figure 10: Thermal via array (left) vs. copper coin (right)

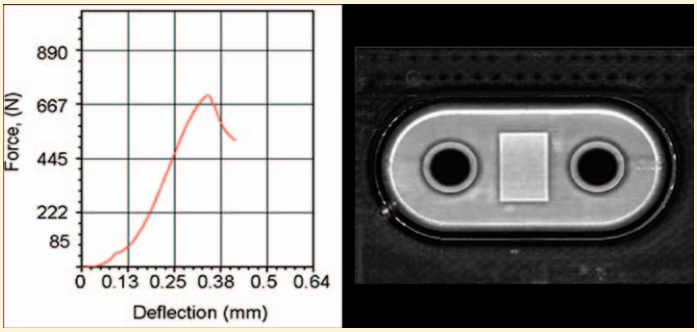

Figure 11: a) Push-out force (left), b) sonic scan (right)

ped. The highest level of precision can be achieved when the copper coins are inserted in a sequential order, coin by coin. This process can be done fully automated and the force that is provided during the coin insertion can be controlled and monitored for each individual coin.

How well the press-fitted copper coins are fastened in the PCB or the bond strength of the adhesive bonded copper coins is measured by the so called push-out test, a test that has been especially developed for the copper coin technique (Figure 11a). This test is typically done before and after some thermal stress. It also can be performed with PCBs at some elevated temperature to prove the condition at operating temperature for example. The quality of the bonding layer on adhesive bonded copper coins is checked in addition with ultra sonic scans (Figure 11b).

The printed circuit boards have to pass several extensive reliability and stress tests before they are released for customer applications. In some cases FEM simulations are supporting this phase of product development. Table 2 lists some typical reliability tests that printed circuit boards with copper coins must pass.

Summary

The integration of copper coins for heat dissipation into the structure of printed circuit boards is a proven and reliable technique. It provides a highly efficient way to dissipate heat from electronic components.

Various methods and techniques have been developed to provide the circuit designer flexibility in terms of board design and choice of materials. The advantage over thermal via arrays has been demonstrated.

The method of press-fitted copper coins is the most attractive solution for the industry because the implementation is very simple and does not require much effort, the costs are very reasonable. If larger coins are needed then some alternative methods such as adhesive bonded coins and embedded coins can be used.

The principle of integrating coins into the PCB construction is also suitable for bare die attachment, providing a much lower thermal resistance in the thermal pathway.

All of these techniques are established methods and are being already applied in a wide range of applications. They can be found in automotive electronics, industrial electronics, and in telecom infrastructure as well as in defence and avionics systems. Just recently press-fitted copper coins have been designed into the rigid section of rigid-flexible circuit board as well. ◄

Machine-to-Machine Applications with Industry Leading Cellular Engines

Skyworks Solutions, Inc. announced that its SkyOne Ultra 2.5 and diversity receive (DRx) modules for mobile applications have been adopted by some of the world's leading machine-to-machine (M2M) module manufacturers to provide high performance, high speed 4G LTE capability. These fully integrated and tested systems, packaged in extremely small form factors, enable M2M suppliers including Fibocom, Sierra Wireless, and Telit to extend plug and play, high-speed cellular connectivity across an endless array of Internet of Things (IoT) products and applications – in any global region and on any wireless network.

SkyOne Ultra 2.5 covers over 20 LTE frequency bands in a complete front-end solution; inclusive of power amplification, duplex filtering and antenna switching. Skyworks' DRx improves receiver sensitivity and cell edge performance while addressing all major downlink carrier aggregation combinations. This highly differentiated solution integrates low noise amplification, receive filtering, and band switching. By supporting global and regionally optimized SKUs in the same PCB footprint, these platforms uniquely enable cost-effective, high performance architectures with ultimate flexibility. According to a recent Cisco VNI report, M2M will be one of the fastest growing mobile connection vehicles as global IoT applications continue to gain traction in consumer and business environments. Cisco forecasts that globally, M2M connections will grow from 780 million in 2016 to 3.3 billion by 2021, at a compounded annual growth rate of 34 percent. Further, M2M mobile connections will exceed a quarter of total devices and connections by 2021, as devices evolve from 2G to 3G, 4G and higher technologies.

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