Design

# Designing a Modified Three-Level Doherty Amplifier for Use in Next-Generation Communication Systems

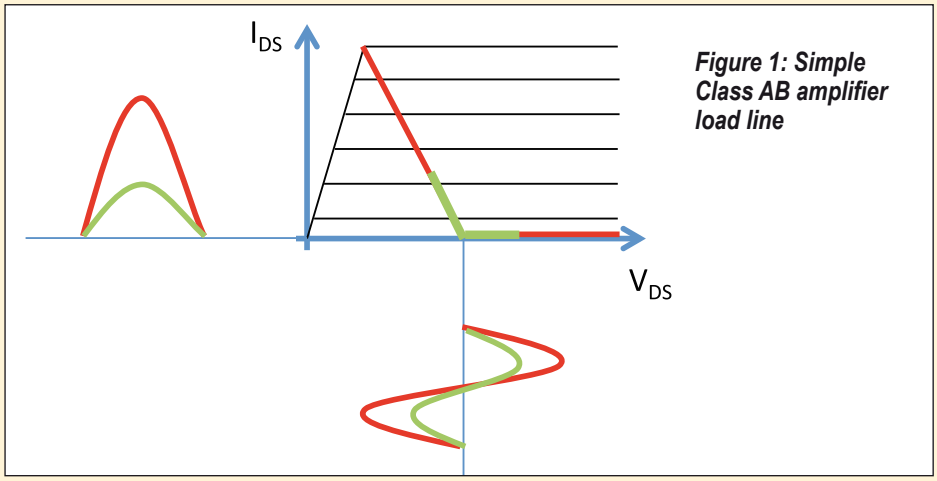


*Figure 1: Simple Class AB amplifier load line*

Today's communication systems often use complex modulation techniques with peak-to-average ratio (PAR) signals of 9 dB and higher, requiring power amplifiers (PAs) in these systems to operate below the power levels that would yield optimum power-added efficiency (PAE). This application note presents an overview and explanation of the operating principle of a modified three-level Doherty that produces good efficiency over the top 10 dB of operation using devices of equal periphery. Design challenges faced with this type of amplifier will be discussed and compared against a conventional three-way Doherty architecture.

One of the simplest forms of RF amplifiers is the Class AB type shown in Figure 1. Such an amplifier is relatively straightforward to design and manufacture and can easily provide peak drain efficiencies of around 65 percent when operating in the 2 GHz region. One drawback with this type of simple amplifier is that when the RF output signal level is reduced, the output voltage swing also reduces and efficiency drops away with the square root of the output power. This means that at a quarter of the output power (-6 dB), the efficiency drops to about half of the output power and half of the peak, 32 percent in this example. Clearly, operating at 6 dB back off and higher with a Class AB amplifier results in a significant reduction in efficiency because the signal is, on average, sitting at a highly inefficient operating point.

The use of Doherty amplifiers is a well-known technique for improving efficiency of a PA in a backed-off operation. The standard two-way Doherty amplifier with a peak in efficiency at 6 dB back off and full power is commonly used and well understood. With the use of increasingly complex signals comes the challenge to move the peak in efficiency to higher levels of back off while maintaining efficiency up to full-power output. This can be achieved with asymmetrical Doherty amplifiers or by utilizing N-way Doherty techniques. This is why the use of Doherty amplifiers in modern code division multiple access (W-CDMA) and long-term evolution (LTE) systems has seen a strong resurgence.

The two-way Doherty provides an improvement over the Class AB case, but with higher levels of PAR being used, it is necessary to improve efficiency at back-off levels of 10 dB and higher. The three-level Doherty produces peaks in efficiency at 9.5 dB, 4.4 dB, and 0 dB, which is a good fit for LTE transmitters, but, as will be seen later, requires that the two auxiliary amplifiers be twice the periphery of the main amplifier.

This application note examines the operation of a modified three-level Doherty [1] that produces good efficiency over the top 10 dB of operation using devices of equal periphery. The operation of the three-level Doherty architecture is explained based on an Ampleon (formerly NXP) design that uses three laterally diffused metal oxide semiconductor (LDMOS) transistors of equal size. Design challenges faced with this type of amplifier are presented and compared against the conventional three-way Doherty architecture. Test results are presented that demonstrate a drain efficiency of greater than 40 percent at 10 dB back off.

The entire RF design, including layout, was implemented in NI AWR Design Environment, specifically Microwave Office circuit design software and APLAC harmonic balance, which were used to simulate in detail the large-signal effects of the Doherty amplifier's operation. The software's load-pull analysis was used to determine the impact of load impedance on amplifier performance.

## The Two-Way Doherty

Although well documented in the literature, it is worth taking a moment to revisit the simple case of the two-way Doherty amplifier to fully understand the three-level con-

*National Instruments*
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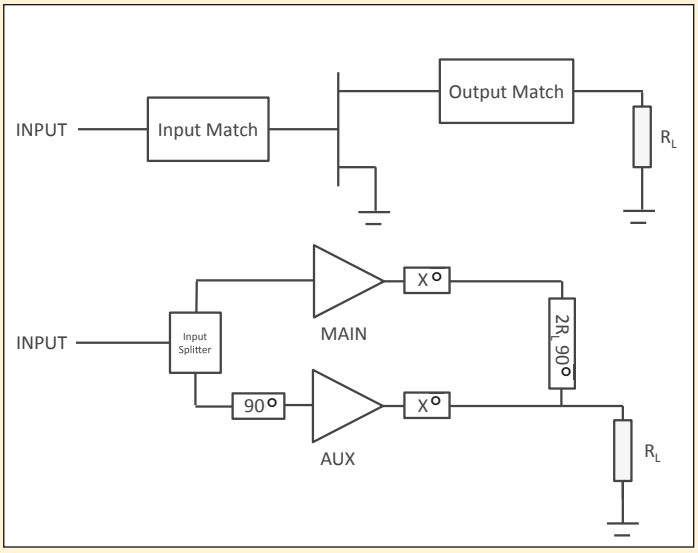


*Figure 2: Single-ended Class AB amplifier (top) and two way Doherty amplifier (bottom)*

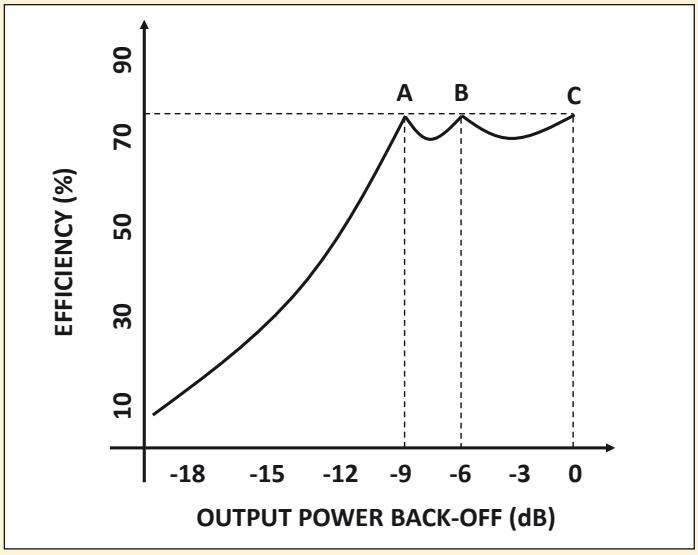


*Figure 3: Three-way Doherty theoretical efficiency curve*

figuration. The standard two-way Doherty amplifier works by splitting the amplifier into two equally-sized amplifiers that are half the size of a single-ended Class AB amplifier with the same peak power capability (Figure 2). The basic principle is that when the output signal level is low, only the main amplifier is active. With increasing output levels the auxiliary amplifier is progressively introduced up to the point where full power is achieved and both the main and auxiliary amplifiers are contributing equally to deliver full power.

The two-way circuit is configured with the main amplifier biased in Class AB and the auxiliary amplifier biased in Class C. This biasing scheme means that at low input drive levels, the main amplifier conducts and the auxiliary amplifier is off. As input levels are increased, the main amplifier drive level also increases and when the output power is a quarter (-6 dB) of the amplifier maximum, the auxiliary amplifier starts to conduct current.

At low signal levels when the auxiliary amplifier is not active, the main amplifier (assuming RL = 25 Ω) "sees" 100 Ω. This means that it reaches full voltage swing at half power. Full voltage swing means that the main amplifier provides maximum efficiency at half its output power. At this point, the amplifier as a whole is delivering a quarter (-6 dB) of its peak power capability with maximum efficiency. This is the first point on the theoretical efficiency curve in Figure 3.

As input drive level is increased from the 6 dB back off point, the current contribution into the load from the auxiliary increases. This increased current being injected by the auxiliary means that the impedance looking into the load increases. The 50 Ω impedance inverter between the load and the main amplifier ensures that the main amplifier sees a reduced load as the current contribution from the auxiliary increases. So, in this regime, as output power increases, there are two processes taking place. The first is that, due to the load modulation from the auxiliary, the main amplifier is effectively increasing in size, that is, it's capability to produce power is increasing during the time it is running at maximum voltage swing and hence maximum efficiency.

The other process that is taking place is that both the main and auxiliary amplifiers are contributing to the total output power. As the drive level increases, these processes continue to increase until the auxiliary is at maximum output power (if devices are equal in size) and the currents into the load from the main and auxiliary are equal. At this point the main and auxiliary amplifiers both see 50 Ω. The key concept in the operation of the Doherty is load modulation. The explanation given in [2] provides an excellent description of the principals involved and the key elements are repeated in this article for clarity.

Figure 4 represents the simplest possible case where two current sources are feeding into a common load. When $I_2 = 0$, then the impedance Z is simply equal to RL. If a current is injected into the load from $I_2$ then the impedance Z is modified to:

Equation 1

$$Z_1 = \left(1 + \frac{I_2}{I_1}\right) R_L$$

If $I_1$ and $I_2$ are equal, then

$Z_1 = Z_2 = 2R_L$

With the addition of an impedance inverter as shown in Figure 5, this circuit becomes the two-way Doherty. The addition of the inverter causes the impedance seen at the main amplifier $Z_m$ to reduce when the current from the auxiliary is injected into the

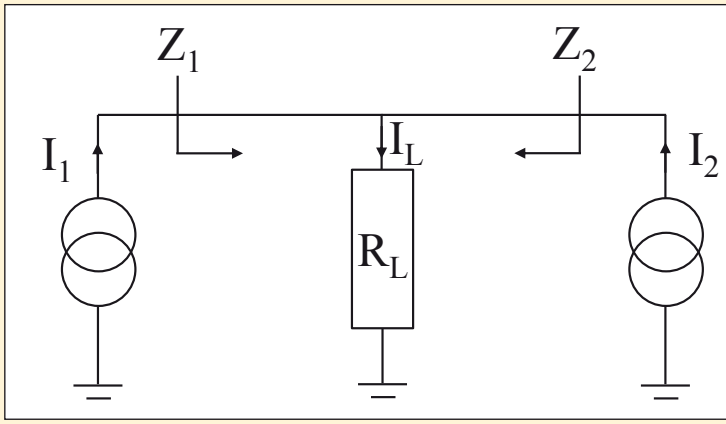


*Figure 4: Standard two Doherty load modulation (inverter removed)*

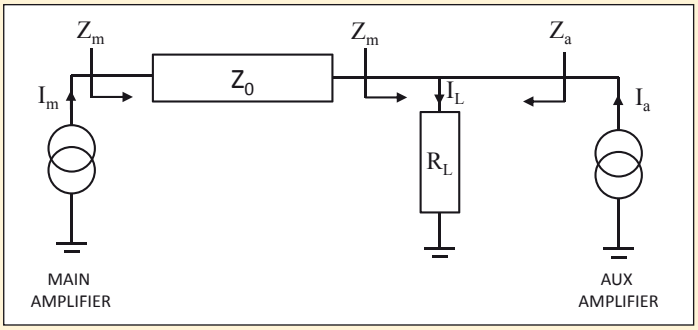


*Figure 5: Two-way Doherty schematic*

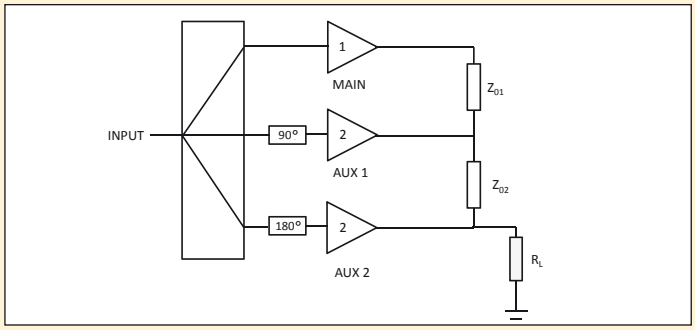


*Figure 6: Conventional three-level Doherty*

common load. When the auxiliary is off then $Z_m = Z_2 / R_L$.

## The Conventional Three-Level Doherty

The conventional three-level Doherty is a direct extension of the two-way design, as shown in Figure 6. By adjusting the relative device periphery between the main and auxiliary amplifiers, it is possible to achieve a variety of different positions for the efficiency peaks. The designer can use the equations defined in [3] to locate the efficiency peaks as required. This article is concerned with signals around 10 dB of PAR. The relative levels of device periphery to achieve an efficiency peak at -9.5 dB, -4.4 dB, and 0 dB for the conventional three-level Doherty is 1:2:2, where the first digit is the main amplifier followed by Aux 1 and Aux 2.

For this configuration, $Z_{01}$ is required to be 70.7 Ω, $Z_{02}$ = 33.3 Ω, and $R_L$ = 20 Ω. At the first efficiency peak the main amplifier will see an impedance of 90 Ω. In order to match the output to 50 Ω, an impedance inverter with a value of √(20 x 50) = 31.6 Ω is required.

In essence, the conventional three-level Doherty behaves as a two-way Doherty up to the second peak (-4.4 dB) in efficiency and then from the second peak to full power the main and Auxiliary 1 amplifiers are behaving like a main amplifier that is being load modulated by the current contribution from Auxiliary 3.

However, there are two main drawbacks of the conventional three-level Doherty. The first is that different device sizes are required to provide efficiency peaks in the 10 dB back off region, which leads to added complexity. The second is that the load modulation of the main amplifier stops between the second and final efficiency peaks. This means that the main amplifier is driven into extreme saturation over the last 6 dB of output power [1].

## Modified Three-Level Doherty With Equal-Sized Devices

The modified three-level Doherty design [1] achieves similar performance to a conventional three-level Doherty, but without having to accommodate output transistors of different sizes. Using transistors of equal sizes for the main and auxiliary stages has a number of practical benefits, including the use of a single "unit cell" RF design. The basic amplifier unit cell for the main and auxiliaries can be of the same (or very similar) design, which reduces development time. Also, having three of the same parts rather than two different parts on the bill of materials results in economies of scale, which is important for what are likely to be the most expensive components in the amplifier. The configuration also provides proper load modulation of the main amplifier, whose load impedance steadily reduces as drive level is increased.

A schematic diagram of the modified three-level Doherty is shown in Figure 7. The best way to understand the operation is to start at low signal levels, progressively increase the input drive level, discuss the operation at each efficiency peak, and refer to the efficiency curve in Figure 3.

Each unit cell in this example delivers maximum output power when driving a 50 Ω load. The unit cell also contains phase offset lines to ensure that the electrical length of an auxiliary (and main) stage is 180 degrees from the active device to the point at which the amplifier is connected into the Doherty combiner circuit. This ensures that when the auxiliary amplifier is switched off, an open circuit is presented to the Doherty combiner and the minimum power is dissipated in the auxiliary output matching circuits. The main amplifier is biased in a Class AB mode, Auxiliary 1 is biased at about 0.7 V, and Auxiliary 2 is biased at about 0 V when using enhancement mode LDMOS transistors. These values provide the required progressive switching of the auxiliary amplifiers. Note that the load value is 16.66 Ω in this example and is transformed up to 50 Ω with a 28.8 Ω quarter-wave inverter.

At low signal levels, in the regime before Point A is reached, only the main amplifier is active. The impedance presented to the main amplifier unit cell at this point is

| Stage | Impedance Presented to Unit Cell | Power Delivered into Output Load. |
|---|---|---|
| Main | 150 Ω | 33% of $P_{MaxMain}$ |
| Aux 1 | Open | 0 |
| Aux 2 | Open | 0 |
| Total Power in Load | | 11% of $P_{Total}$ |
| Power Delivered/Total Power Capability (Backoff Level in dB) | | 10Log(0.33/3) = -9.6dB |

*Table 1: NODE A*

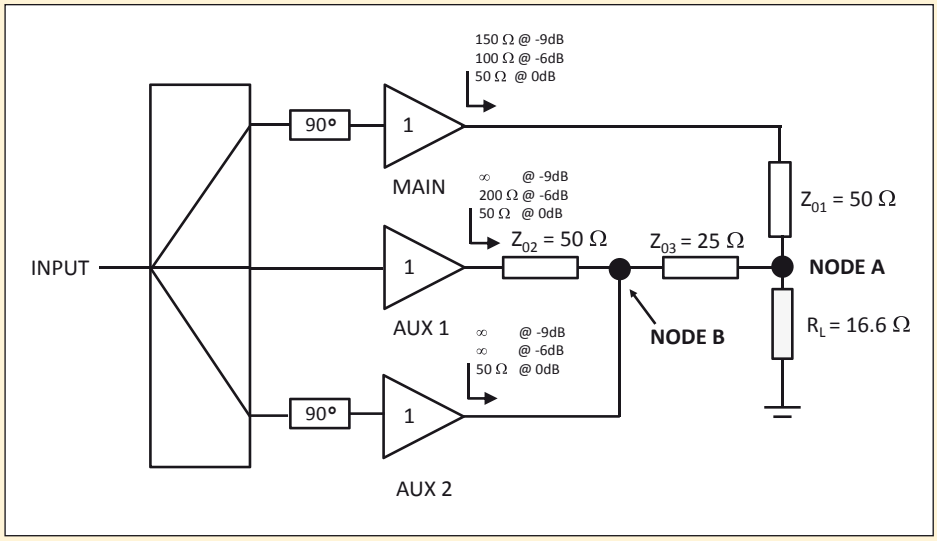


***Figure 7: Modified three-level Doherty schematic***

150 Ω. At NODE A, the conditions shown in Table 1 apply.

As the input drive level increases, it moves to the region between Point A and B in Figure 3. At Point A, Auxiliary 1 switches on and starts to deliver current into the common output load $R_L$. This increase in current in the common load causes the impedance seen from the main amplifier at Node A to increase. The action of the inverter $Z_{01}$ in the main path causes the impedance seen by the main amplifier to fall. This reduction in output impedance enables the main amplifier to deliver more power into the common load whilst remaining in voltage saturation.

As drive level is increased, this process continues until the current in the load due to the auxiliary is half that of the current in the load due to the main, and the following condition is reached:

Equation 2

$$\frac{I_{A1}}{I_M}=0.5$$

This condition is Point B in Figure 3 and is the second efficiency peak. At this point, applying Equation 1, the impedance seen from the main amplifier looking into Node A is given by:

Equation 3

$$Z_{M\_NodeA} = R_L\left(1+\frac{I_{A1}}{I_M}\right)=\frac{3}{2}R_L = 25\Omega$$

So, the impedance seen by the main device looking into 50 Ω inverter $Z_{01}$ is 100 Ω Also, the impedance seen from the auxiliary branch looking into Node A is given by:

Equation 4

$$Z_{A\_NodeA} = R_L\left(1+\frac{I_M}{I_{A1}}\right) = 3R_L = 50\Omega$$

The impedance at Node B looking from Auxiliary 2 is therefore 12.5 Ω (due to $Z_{03}$) and the impedance seen by the Auxiliary 1 unit cell amplifier is 200 Ω. Since the main amplifier and Auxiliary 1 are both running at voltage saturation, they both deliver maximum efficiency, hence the peak in efficiency. The parameters for the amplifier at this second efficiency peak are given in Table 2.

The bias of Auxiliary 2 is set such that it starts to turn on and deliver current into the output load when Equation 2 is satisfied. The increase in current further reduces the main impedance and allows it to deliver more power. The increased current into the load also reduces the load impedance seen by Auxiliary 1, so this device delivers more power and further increases load current. This increase in current continues until the contribution from each amplifier is equal and the following is satisfied:

Equation 5

$$I_M = I_{A1} = I_{A2}$$

The two auxiliaries deliver a total normalized current of 2 into the load and the main delivers 1. This is Point C in Figure 3. At this point, the impedance from the main branch looking into Node A is now:

Equation 6:

$$Z_{M\_NodeA} = R_L\left(1+\frac{I_{A1+1A2}}{I_M}\right) = 3R_L = 50\Omega$$

The main amplifier sees 50 Ω and delivers full power. The impedance seen from the auxiliary branch looking into Node A is given by:

Equation 7:

$$Z_{A\_NodeA} = R_L\left(1+\frac{I_M}{I_{A1}+I_{A2}}\right) = \frac{3}{2}R_L = 25\Omega$$

Since $Z_{03}$ is a 25 Ω inverter, the impedance looking into Node B is also 25 Ω. This is the correct impedance for two 50 Ω loads in parallel. The parameters for the amplifier at this third and final efficiency peak are given in Table 3.

In addition to the design of the output network, there are a number of practical design considerations of this type of amplifier that should be considered. The first is that the gain of the three-level amplifier is inherently quite low because of the three-way input split. This results in the small-signal gain being a minimum of 4.7 dB lower than that obtained from a single ended device. This is less of an issue at lower cellular bands, but can become a problem at higher frequencies where gain is at a premium. The quarter-wave transformers used extensively in this design limit the bandwidth to about four to five percent maximum, so is only currently applicable to narrowband applications.

| Stage | Impedance Presented to Unit Cell | Power Delivered into Output Load |
|---|---|---|
| Main | 100 Ω | 50% of $P_{MaxMain}$ |
| Aux 1 | 200 Ω | 25% of $P_{MaxAUX1}$ |
| Aux 2 | Open | 0 |
| Total Power in Load (Max = 3) | | 25% of $P_{Total}$ |
| Power Delivered/Total Power Capability (Backoff Level in dB) | | 10Log(0.75/3) = -6.0 dB |

***Table 2: Parameters for the amplifier at this second efficiency peak***

| Stage | Impedance Presented to Unit Cell | Power Delivered into Output Load |
|---|---|---|
| Main | 50 Ω | 100% of $P_{MaxMain}$ |
| Aux 1 | 50 Ω | 100% of $P_{MaxAUX1}$ |
| Aux 2 | 50 Ω | 100% of $P_{MaxAUX2}$ |
| Total Power in Load (Max = 3) | | 100% of $P_{Total}$ |
| Power Delivered/Total Power Capability (Backoff Level in dB) | | 10Log(1) = 0 dB |

*Table 3: Parameters for the amplifier at this third and final efficiency peak*

## A 2.14 GHz Three-Level Doherty

In order to demonstrate the concept, a 2.14 GHz version of the Ampleon three-level amplifier was designed and manufactured by Slipstream Engineering Design. A photograph of the amplifier is shown in Figure 8.

The three-way input splitting (-4.7 dB) is achieved by using a 5 dB directional coupler cascaded with a 3 dB hybrid coupler. The transistors used are twin LDMOS devices running from 28 V (normally used for push/pull or balanced applications) with one of the transistors not used in the upper device. Results are presented as back off levels from full output power, which in this case is classed as around 2 dB output compression. As can be seen, the design objective of 40 percent drain efficiency at 10 dB back off has been achieved over the band of interest. Although not shown here, the small-signal gain of this amplifier was about 16 dB, with a power gain at full power of 14 dB. Figure 9 shows the continuous wave test results for the Ampleon amplifier at full power of 150 W.

*Figure 8: Slipstream Engineering Design 2,14 GHz three-way amplifier implementing Ampleon Doherty Design*

## Conclusion

This article has presented an overview and explanation of the operating principle of a modified Ampleon three-level Doherty [3] that produces good efficiency over the top 10 dB of operation using devices of equal periphery. Design challenges faced with this type of amplifier have been presented and compared against conventional three-way Doherty architecture. Experimental results of a fabricated amplifier have been presented that demonstrate a drain efficiency of greater than 40 percent at 10 dB back off. ◄

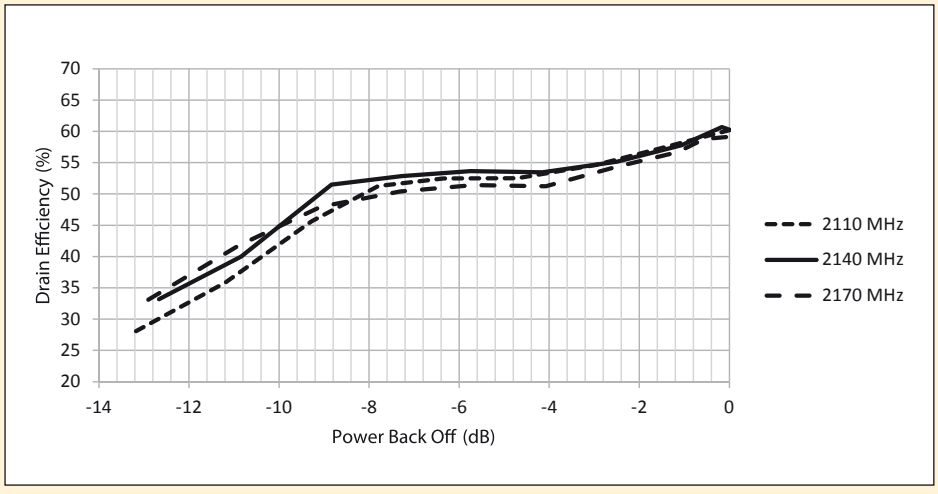


*Figure 9: Ampleon amplifier continuous wave test results of 150 W*

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