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Test & Measurement

Multi-Chip module design, verification, and yield optimization

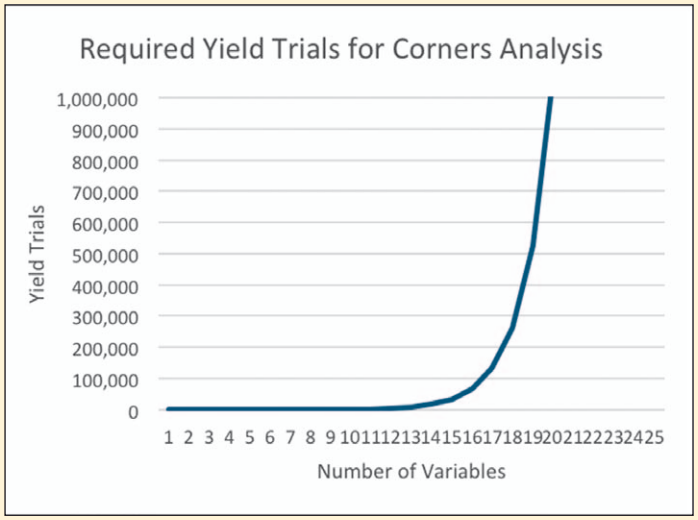

Figure 1: Corners analysis for a yield analysis with many variables is impractical because the number of yield trials grows exponentially with the number of variables

As wireless communications systems evolve, smaller devices with better performance are required that incorporate multi-technology-based module designs with different integrated circuit and printed circuit board process technologies. Front-end module manufacturers are now integrating gallium arsenide (GaAs), silicon germanium (SiGe), or radio-frequency complementary metal-oxide semiconductor (RF CMOS) power amplifiers, CMOS or silicon-on-insulator (SOI) switches, and acoustic filters - all mounted on a single laminate package.

This application note presents a unified design flow that streamlines full module simulation, inclusive of all process technologies, enabling designers to leverage the strengths of specialized electromagnetic modeling and circuit analysis tools to address various functional block technologies, maintaining all through a single user-interface environment. The application is a dual band, 1.9 GHz (cellular)/ 2.5 GHz wireless local area network WLAN-FEM that includes two PAs (GaAs and SiGe), surface-mount bulk acoustic wave (-BAW) filters, and a laminate substrate.

The designer used full-design simulation, inclusive of EM verification and yield optimization, enabling him to not only understand the design sensitivity to specific component and manufacturing tolerances but also to compensate for the impact of these variations on the overall design performance in order to achieve a more robust end product.

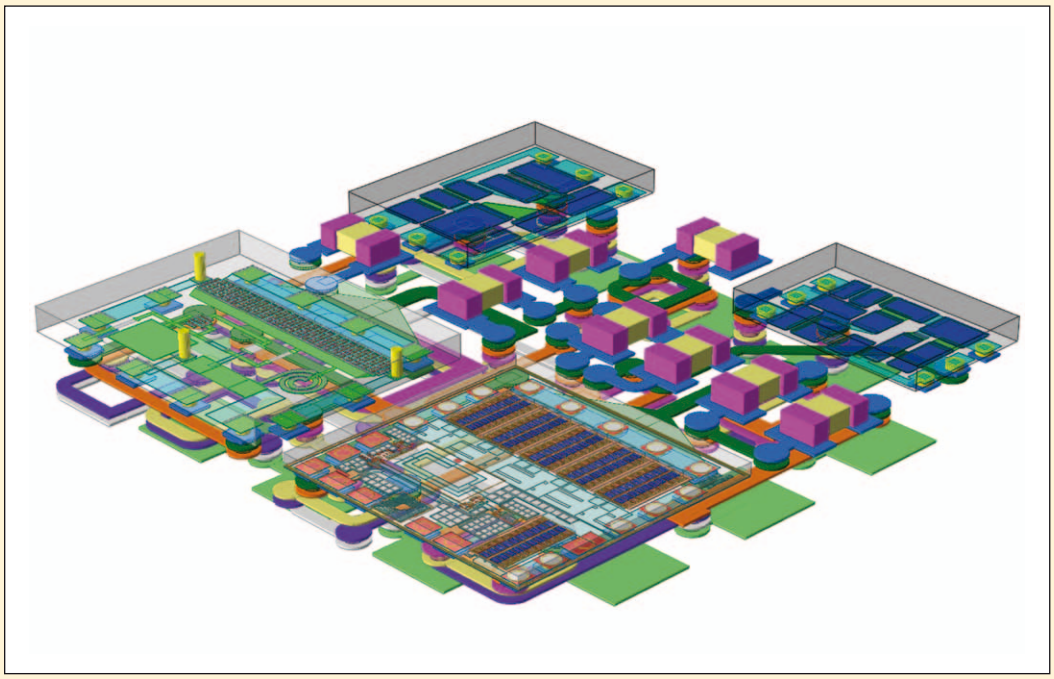

Figure 2: In module design there are usually multiple technologies, as well as the PCB technology of the module itself

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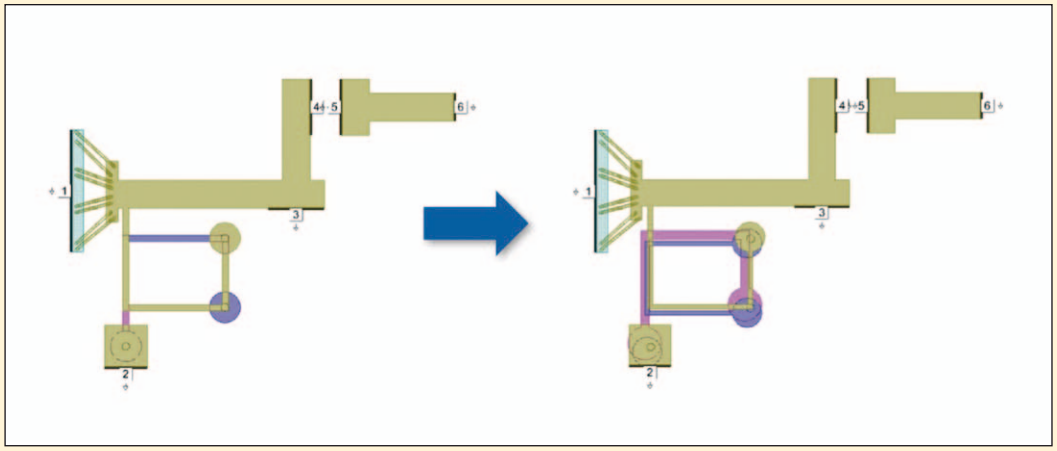

Figure 3: In the spiral inductor on the left, the metals are all the same width and are aligned on the Z axis, while on the right the layers have shifted in X and Y independently of one another

Multi-Chip Module Design Issues

Multi-chip module designers face a multitude of design challenges relating to the manufacturability of complex multi-layer substrates. Included in these challenges are many uncorrelated factors associated with substrate fabrication such as registration errors or etch-tolerance of the package trace metals. While a corners analysis would be a typical process for IC design, doing it for yield analysis of a module with a large number of variables becomes impractical very quickly, as the number of yield trials required grows exponentially with the number of variables (Fig. 1).

For example, consider a five-layer module with 10 surface-mount components. Here there might be five variables each for registration, under/over etch, and dielectric variation, as well as 10 variables for the variation of the surface-mount parts, resulting in 33.55 million yield trials. No reasonable designer could wait for the simulation results for such a large amount of simulation trials.

Another challenge concerns capturing the component-to-component interactions in a module design that often contains multiple technologies that are analyzed with separate, specialized IC- and PCB-focused simulation tools/design flows (Fig. 2).

While designers rely on tools that are efficient for designing each constituent part of the module, at some point in time, they do need to bring all of these disparate designs together in order to perform a full system simulation and verification. If the component tools are interoperable, designers are able to quickly simulate and verify the full system design more readily. A simple example of this would be a case where a silicon chip (RFIC) is designed using a Cadence tool and the PCB is designed with NI AWR Design Environment, specifically Microwave Office circuit design software.

Microwave Office Design Flow

To address these challenges, Microwave Office software offers an integrated design flow for harnessing multiple simulation technologies developed specially to address individual components found in multi-chip module design. Tool interoperability between NI AWR Design Environment and third-party specialized tools allow designers to incorporate existing IC designs represented as blocks within the overall multichip/substrate simulation. In the example discussed above, the RFIC was imported as a Cadence-generated Spectre circuit simulator netlist into NI AWR Design Environment, which then directly simulated the Spectre netlist block using the APLAC harmonic balance / transient circuit simulation engine.

Designers can therefore turn their attention to optimizing off-chip design, interconnect, and matching network modeling, as well as yield or corners analysis. Design centering for improved yield analysis can also take place through surface-mount component selection or laminate redesign directly in Microwave Office.

Alternatively, a parameterized Spectre netlist containing S-parameter data sets from the yield analysis can be exported from the NI AWR Design Environment and used within Cadence to address design centering for higher yields at the RFIC level.

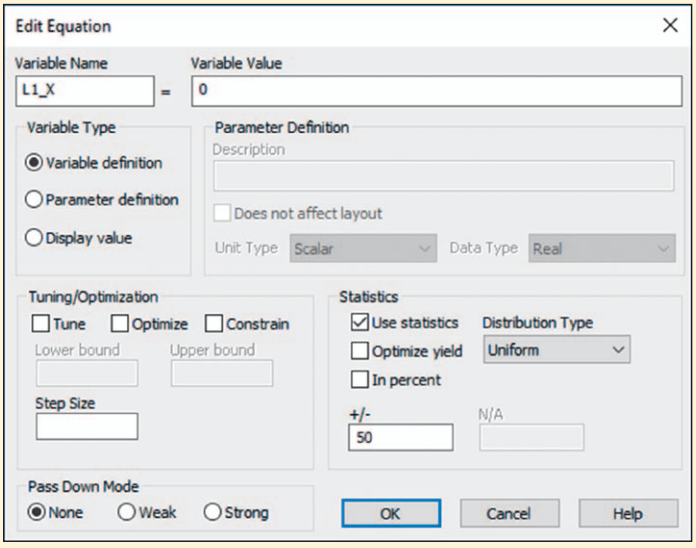

Figure 4: Statistical variation for each layer

To expedite yield analysis with a more efficient alternative than corners analysis, Microwave Office software provides Monte Carlo analysis, which can give meaningful yield results with fewer yield trials. In addition, even though Monte Carlo analysis is more efficient, there will still be a large number of yield simulations that need to be performed, which can be very time consuming. Thus, software such as Microwave Office also provides the ability to distribute and parallelize these simulations among remote servers, thereby further reducing the amount of time it takes for engineers to obtain their yield results.

Monte Carlo Analysis

Monte Carlo yield analysis consists of performing a series of trials or iterations. Each trial results from randomly generating parameter values according to its specified statistical variation, performing a simulation, and evaluating the result against stated performance specifications. It is easy to compute the number of yield trials required to achieve a specific yield percentage with an acceptable error percentage for a particular confidence level.

For example, if the yield is 90 percent, a one-percent error in results is acceptable, and the confidence level is 95.4 percent,

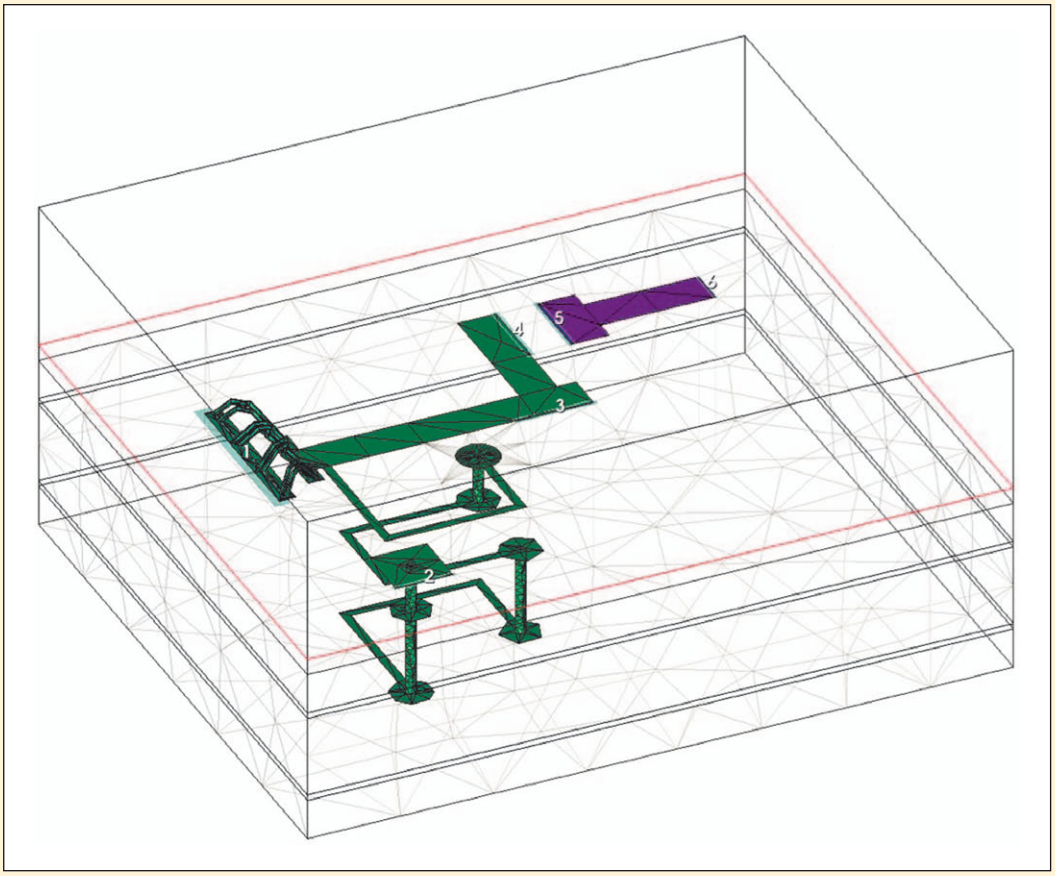

Figure 5: The connectivity highlighter in Microwave Office highlights if the metal connectivity is changing to ensure there are no opens or short in the circuit when using the layer modifiers tool

with the equivalent number of yield trials at 3600, as shown in Equation 1.

$$N = \left(\frac{C_\sigma}{\varepsilon}\right)^2 \cdot Y(1-Y)$$

The sample or trial size, N, is then calculated from:

- Confidence level (standard deviations)
- % error (ε)
- % yield (Y)
- Number of trials (N)

A confidence level of 95.4 percent equals a standard deviation of two, therefore the number of trials is calculated at 3600, or in equation form:

N = (2/.01)^2 x 0.9(1-0.9) = 3600.

Given that Monte Carlo analysis is not a function of the number of variables, the designer can get meaningful yield analysis results for problem spaces with a large number of independent variables with much fewer trials than a corners analysis.

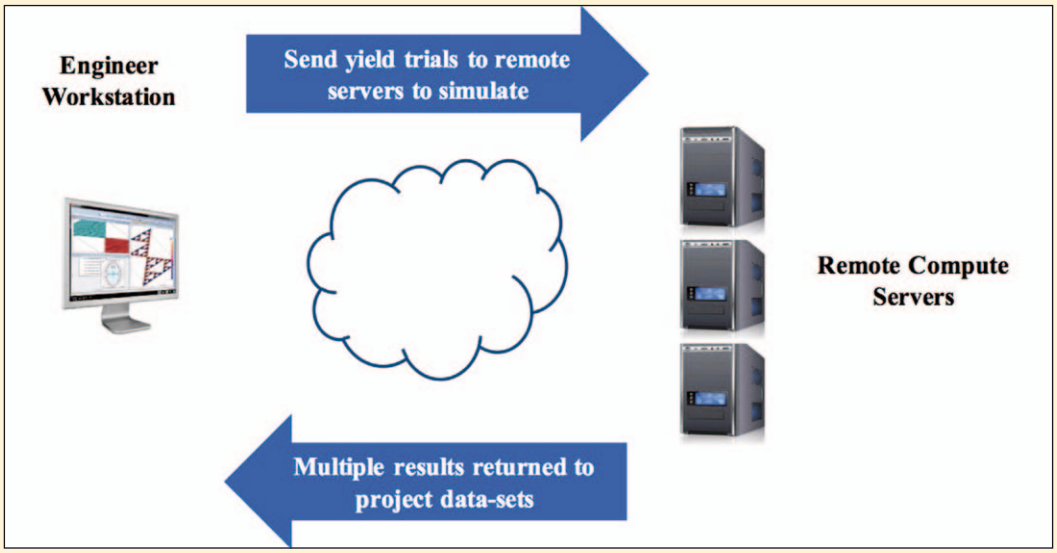

Figure 6: Microwave Office distributed EM capabilities enable users to send all EM simulations to a remote server for parallel simulations, which reduces simulation times and returns results more quickly

Laminate Yield Analysis

NI AWR Design Environment supports the analysis of manufacturing variations, which is especially useful in laminate design. The software offers layer-based modifiers that shift entire layers, making setup very straightforward when looking at the registration error, over/under etch factor, particular manufacturing variations, parametric material dielectric variations, or surface-mount part tolerances. Because they are simply parameters, the designer can do a parametric sweep or set up a particular yield distribution for these parameters. Even more conveniently, the environment provides a viewer with connectivity for visual verification of these geometry modifications.

Layer-Based Shape Modifiers

To elaborate on layer-based shape modifiers, when looking at the spiral inductor on the left in Fig. 3, it can be seen that the metals are all the same width and, in addition, are all aligned with each other in the Z axis. It can be seen that there is no registration error.

In the spiral inductor on the right, however, the layers have shifted independently of one another in the X and Y axis. In addition, the pink one has become thicker and the gold one has become thinner. These issues correspond to the registration error as well as the over/under etch.

For each layer there might be one modifier and then the amount that it moves each layer can be

• Spectre netlist of yield trials

```
//NI AWR Design Environment
//Version 13 build 7997 rev 3
//Export script version: 0.0
//Simulation document name: Spectre_Netlist_Generate_TB
//MDIF name: yield_and_core_thickness

simulator lang = spectre

subckt Spectre_Netlist_Generate_TB (1 2 3)
Parameters
+ L4_THICKNESS=1
+ INDEX=1

if (L4_THICKNESS==1 && INDEX==1) {
```

Figure 7: Microwave Office outputs the results of yield analysis as Cadence-compatible Spectre netlists

assigned a parameter based on a statistical variation, as shown in Fig. 4.

Statistical Parameters

Setting up the statistical variation for the dielectric constant in this module example is also quite easy. The designer need only indicate that this variable is enabled for statistics, specify a distribution type, and assign it a standard deviation or variation percentage. This variable is then used in the material stackup profile. When a yield analysis is performed, the value of the dielectric constant will assume a value based on its statistical variation.

Visual Inspection with Connectivity

When manipulating layers, as is done with the layer-based modifiers feature, incorrect numbers can be entered that result in shorts or opens in the circuit. The connectivity highlighter tool in Microwave Office shows if the metal connectivity is changing, enabling designers to ensure that there are no opens or shorts in the circuit prior to simulation. (Fig. 5).

Distributed Parallel EM Simulations

To speed up simulation run times, the distributed EM capabilities within NI AWR software enable users to send all of the EM simulations to a remote server and distribute those simulations across any number of computers, significantly reducing simulation wait time since the amount of time it takes to get the results back is divided by the number of computers being used for parallel simulations (Fig. 6). The results that come back are in the form of data sets that can be used later.

Cadence Compatible Models

The output of the yield analysis in NI AWR Design Environment is a parameterized Spectre netlist of S-parameters that correspond to the yield analysis trials (Fig. 7). This allows module representation resulting from the yield analysis to be utilized in Cadence for design optimization of the RFIC power amplifier.

Load-Pull Model

Microwave Office-generated load-pull data files can be used in conjunction with yield analysis to study the impact of module manufacturing tolerances on nonlinear behavior using load pull. These load-pull files contain the A and B waves of the device as a function of load and source impedance presented to the device. A and B waves are used to derive other performance metrics of the device, such as power-added efficiency (PAE), gain, and output power. The performance metrics can be interpolated for an arbitrary load presented to the device. This method can be used during yield analysis

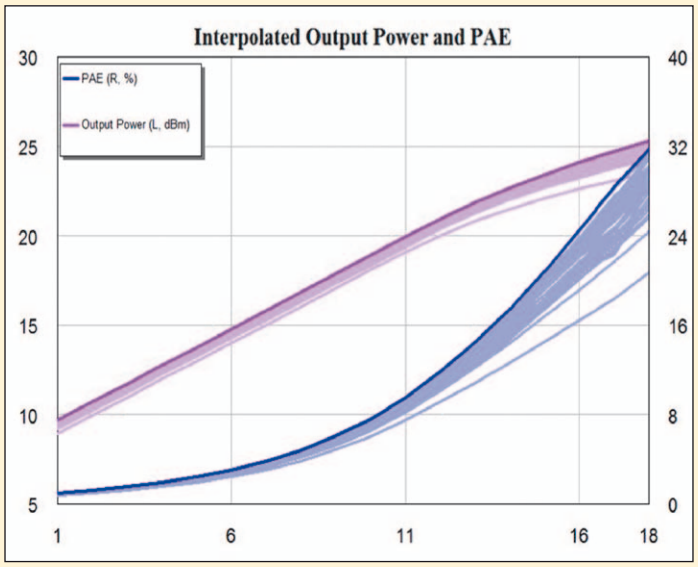

Figure 8: The actual PAE and output power for a yield analysis, where the impedances presented to the device were arbitrary and the output power and PAE were interpolated

	C1	C2	Er	M1 Etch	Cont…
Nominal	1 pF	100 pF	4.47	0 um	…
Outlier	1.28 pF	119.6 pF	4.58	-5 um	…

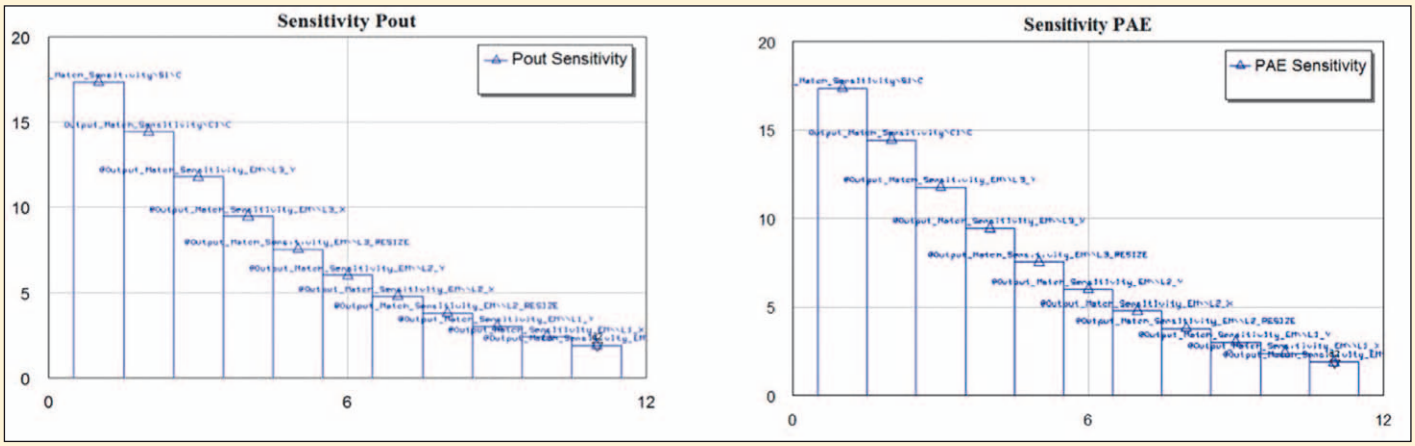

Figure 9: The sensitivity of the output power and PAE are examined over all the variables in that particular yield analysis

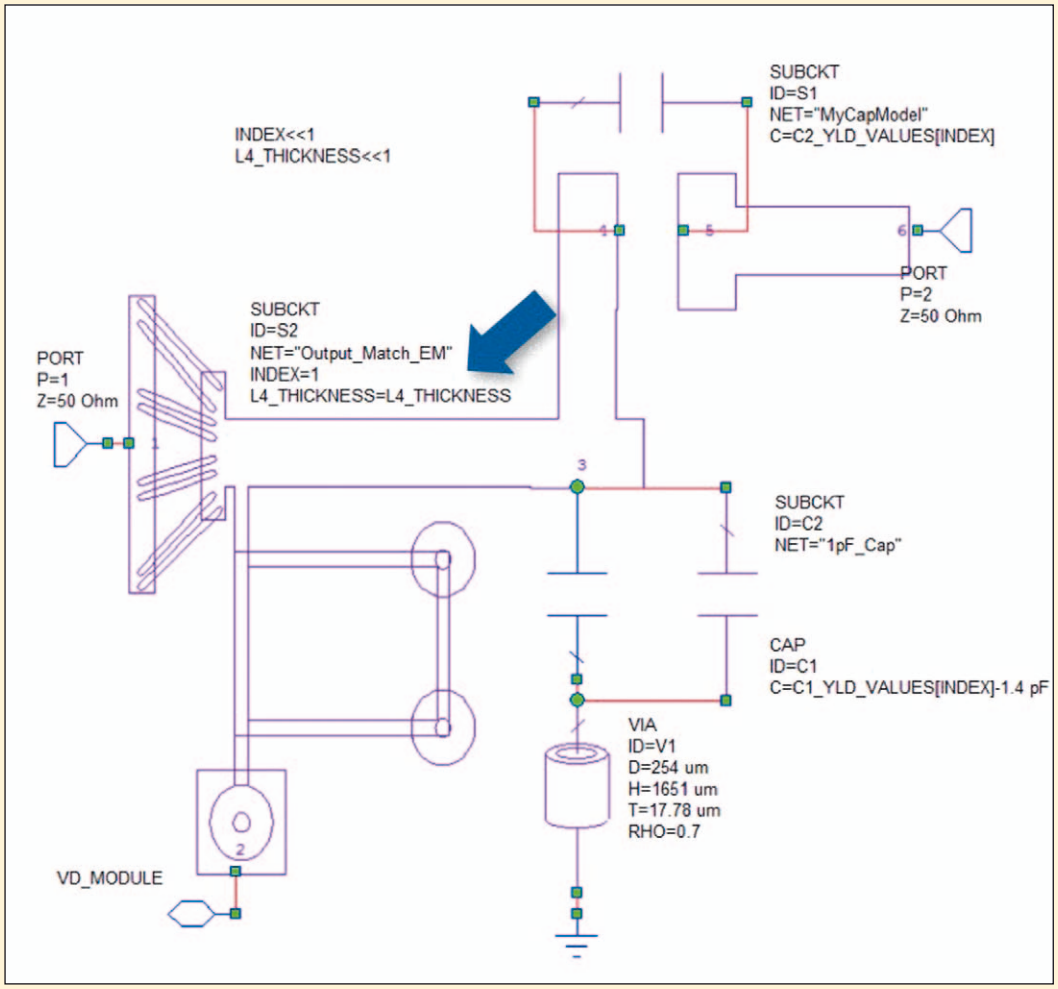

Figure 10: The PCB design can be exported to Cadence, where the IC designer can optimize the PCB to the IC

and is a great way to quickly get circuit performance metrics for arbitrary loads.

This capability enables users to simulate the performance of an active device (transistor or PA) without actually having a device model in the environment, so there is no need to translate the model or have cross-tool process design kit (PDK) support.

In addition, the simulation speed is more like a linear simulation rather than a harmonic balance nonlinear simulation, even though the user is looking at nonlinear results like output power or PAE. When performing a yield analysis, designers are able to leverage the simulated load-pull data, which allows them to apply an arbitrary load and provide the required interpolated performance metrics.

The graph in Fig. 8 shows the actual PAE and output power for a yield analysis where the variations in results are due to changing impedances presented to the output of the chip PA by the laminate, highlighting the interactions that occur between the MMIC/RFIC and module/packaging.

Design Centering

Once the yield analysis is performed, the designer can identify the parameter sets that lead to yield failures or correspond to the outlier traces shown in Fig. 8. Then the tolerances of the yield variables can be changed or the design can be centered so the yield is higher.

Sensitivity Analysis

In addition to yield analysis, NI AWR Design Environment users are able to do a full sensitivity or Pareto analysis. The benefit of this is that all the variables that are set up for yield are weighed against one another, enabling designers to look at which particular parameters in the yield analysis are causing the most change or degradation of particular performance metrics. For example, in Fig. 9 the sensitivity of the output power and PAE are being examined over all the variables in that particular yield analysis, and those variables are going to be different for each performance metric.

Design Methodology Scales to Design Variables

This same methodology corresponds to design as well as yield. The PCB/module designer can perform a parametric design and export it as a parameterized netlist into Cadence, where the IC designer can understand the design constraints and optimize the IC in order to get the best performance out of the total module (Fig. 10). With a parameterized laminate, the IC designer working in Cadence is not constrained to a "fixed" laminate model and can explore different variations within a single, parameterized laminate model block.

Conclusion

This application note has described a unified design flow, inclusive of EM verification and yield optimization, for a front-end module involving several process technologies. Using NI AWR Design Environment enabled the designer to understand sensitivity to specific component and manufacturing tolerances and compensate for the impact of the variations on the overall design performance to achieve design goals of small size and optimum performance.

Because of the large number of independent variables in module design and analysis, it is important to leverage a design flow that can handle yield analysis with many independent variables. The Monte Carlo approach within Microwave Office software provides a more efficient analysis than traditional corners analysis. Microwave Office shape/layer modifiers enables designers to look at the actual manufacturing variances that occur in modules, such as registration error or edge tolerance. In order to minimize simulation time and get results back more quickly,

designers can leverage remote simulation servers in order to take advantage of distributed parallel EM simulation. Finally, by creating Cadence-compatible models and parameterized Spectre netlists, NI AWR software further enables designers to combine simulations and look at the full system simulation and verification. ◄