NI AWR Design Environment Load-Pull Simulation Supports the Design of Wideband High-Efficiency Power Amplifiers

The design of power amplifiers (PAs) for present and future wireless systems requires accurate device models and simulation tools. Manufacturers of high-performance power transistors have invested many hours of research, measurement, and testing in order to have accurate, scalable models.

In most cases, this work has been done in collaboration with the major developers of design and simulation software, who must provide their users with advanced analysis and synthesis functions to support modern design methodologies. The result is a robust set of tools that enables PA designers to optimize input and output matching circuits to obtain the correct device voltage and current waveforms for the desired class of operation.
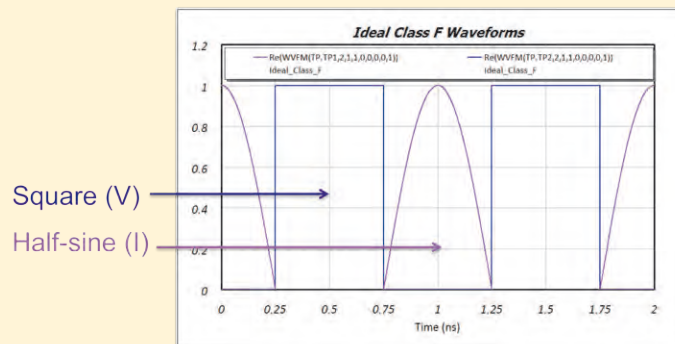

Figure 1: An ideal Class F amplifier will have a square voltage waveform at the drain-source terminal pair and a corresponding half-sine current waveform.

Load-pull simulation is one of the most valuable tools for high-efficiency switch-mode PA design. For these modes of operation (Classes E, F, inverse F, and others), the class of operation is determined by the behavior of input and output matching networks at harmonic frequencies. The PA designer must simultaneously find the most efficient impedance match at the fundamental while properly terminating each harmonic with the necessary short or open circuit. The ability to use load-pull simulation to determine device characteristic impedances at harmonic frequencies greatly speeds and simplifies the design process.

This application note explores the design of power amplifiers using the load-pull scripts that are available in NI AWR Design Environment Microwave Office circuit design software. Using the example of a Cree CGH40010F gallium nitride (GaN) high-electron mobility transistor (HEMT) in a Class F PA at 2000 MHz, this paper demonstrates how power-added efficiency (PAE) is maximized by optimizing source and load pull at the fundamental frequency, plus second and third harmonics ($2f_0$ and $3f_0$).

Fundamental and harmonic load pull using Microwave Office load-pull wizard

An ideal Class F power amplifier will have a square voltage waveform between the drain and source terminals, along with a corresponding half sine current waveform (Figure 1). It is well known that a perfect-square wave contains an infinite number of odd harmonics. In practice, however, only a small number of harmonics can be accommodated within the operating bandwidth of the PA device and its surrounding circuitry. Designers rarely consider more than five harmonics and typically limit rigorous design to three harmonics. With a square-wave approximation using five harmonics, a Class F PA would have a maximum PAE in the 90 percent range. The example in this paper
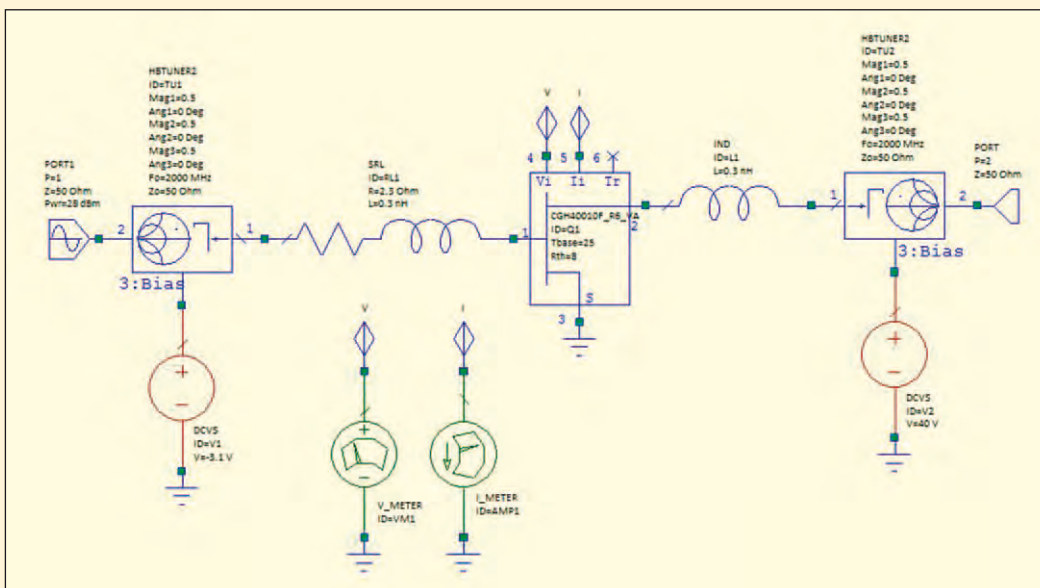

Figure 2: Load-pull Wizard within NI AWR Design Environment - Microwave Office software enables simulation instead of costly, time-consuming bench measurements.
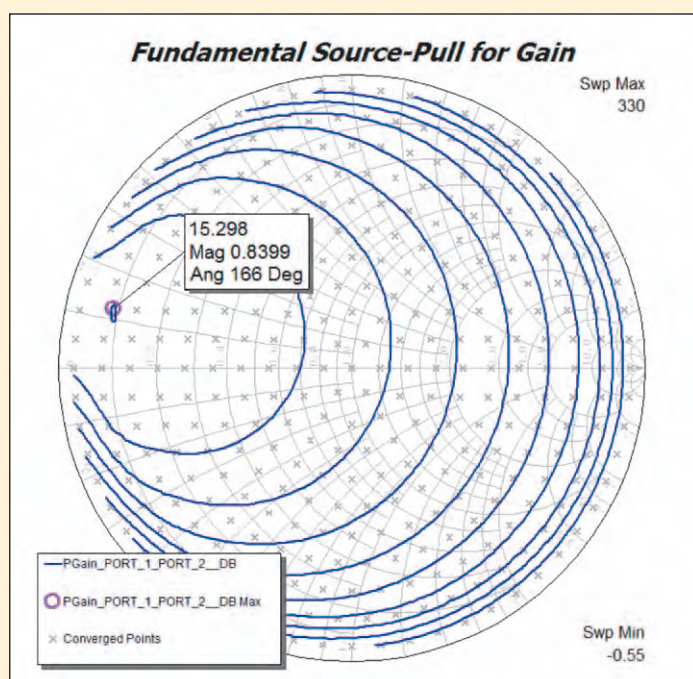
Figure 3: The fundamental frequency source pull for gain.

Figure 4: Maximum power source impedance very close to maximum gain impedance.

is designed using the second and third harmonics.

The NI AWR Design Environment Microwave Office Load-Pull Wizard provides users with an automated process that is much easier than manual methods in the design of networks. Figure 2 shows the basic setup: a source-pull tuner is at the input (left) and a load-pull tuner is at the output (right), with bias Ts integrated into those tuners. The CGH40010F GaN HEMT device is a bare die, so wire bonds have been included to show the effect of additional parasitics on the waveforms generated by the simulation.
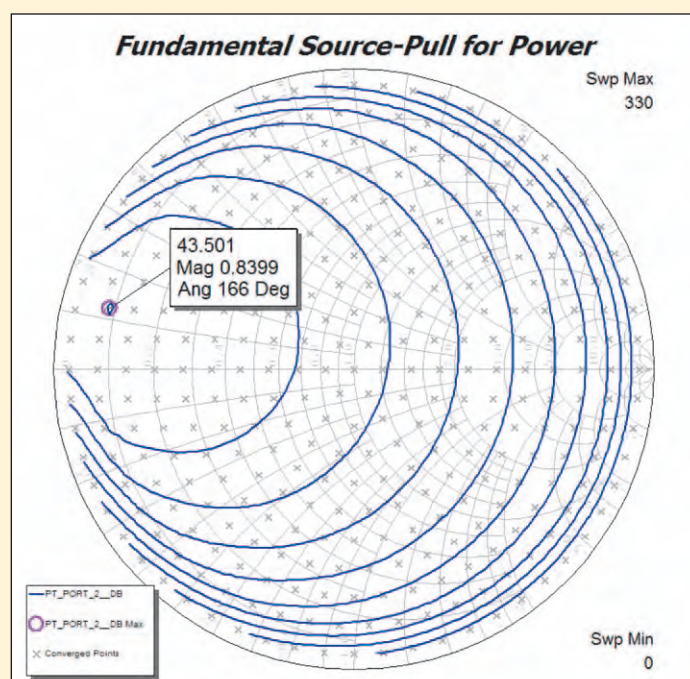
The first step is to do a source-pull simulation for power gain and PAE at the fundamental frequency, where the assumption is made is that the output of the transistor, in this case a bare die, is directly connected to a 50 ohm load. Then the second and third harmonic terminations can be loaded into the load-pull wizard, with their load-pull tuners set to either arbitrary values or to the short and open conditions required for Class F. It will be shown later that because transistors have parasitics, the resulting networks will require some adjustment to obtain the desired
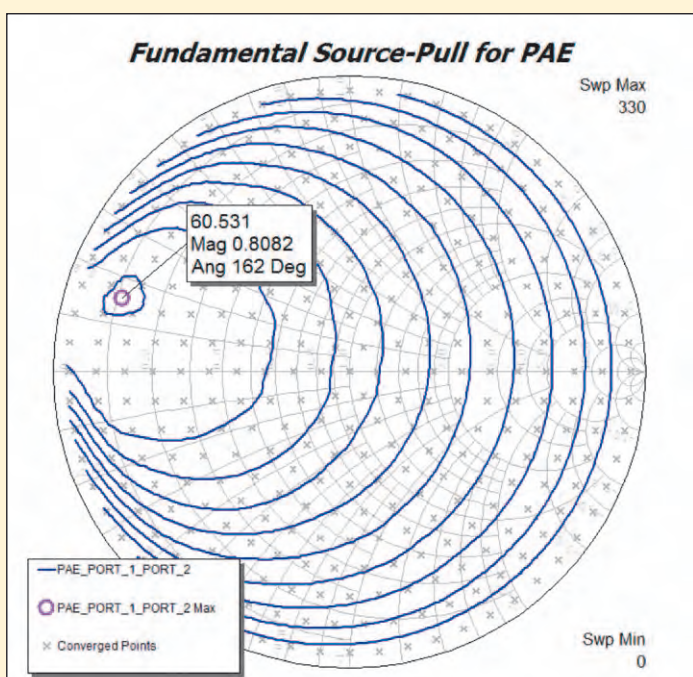

Figure 5: Maximum PAE impedance is very close to maximum for both gain and power, which simplifies the matching task.
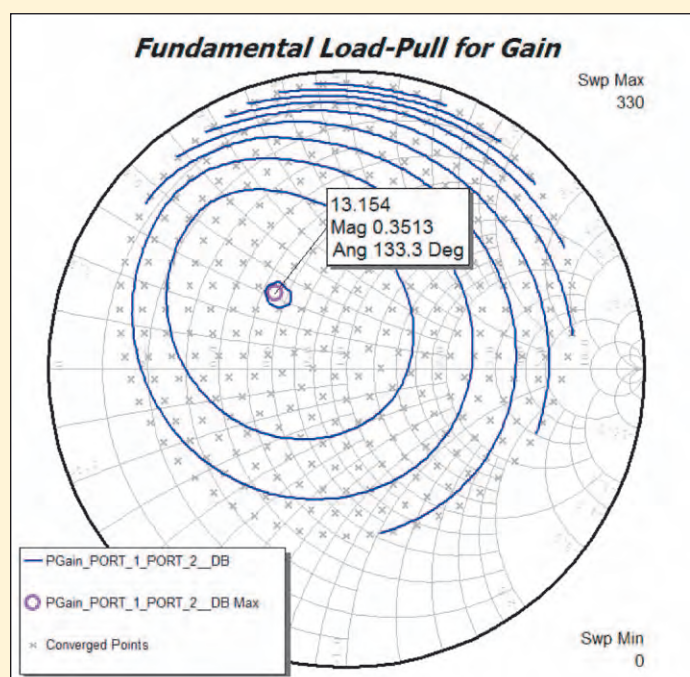

Figure 6: The optimum impedance for gain on the load side of the device is relatively close to 50 ohms
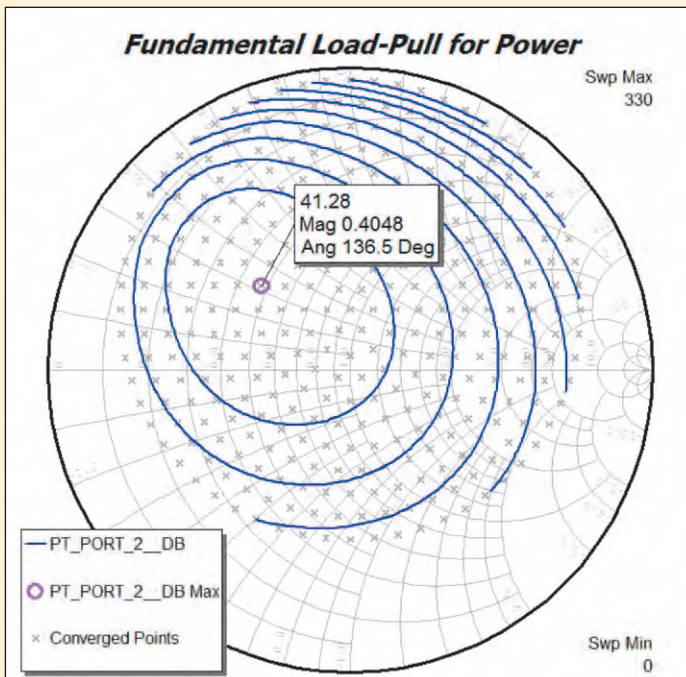
Figure 7: Fundamental load-pull for power, similar to the impedance point for gain in Fig.6
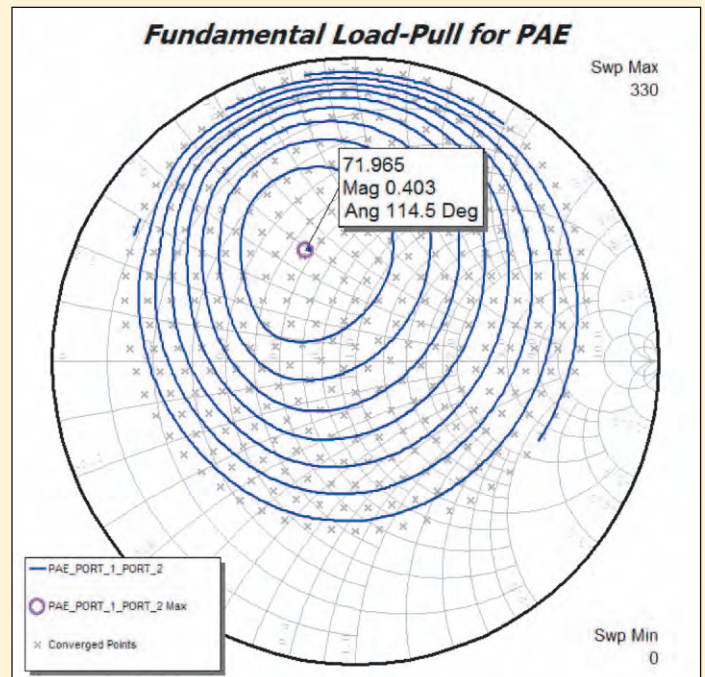

Figure 8: Load pull with the source tuner set for optimal PAE from the impedance point for gain in Fig. 6 source-pull data. PAE improves from 60.5 percent (source pull only) to 72 percent (both ports matched for PAE at fundamental only)

drain-source voltage and current waveforms. This waveform engineering will actually be done via the load-pull wizard to peak up the power, gain, and efficiency. After fundamental frequency source pull has been done with the 50-ohm output load, the next step is to change the setup for fundamental load pull. Again, the goals are power gain and PAE using the optimum input impedance point for each test frequency, as determined by the source pull. Finally, second and third harmonic source pull and load pull will be invoked with the wizard to further improve power gain and PAE, ensuring that the best performance is obtained from the device.

Of course, when second and third harmonic terminations are included, their impedances will likely have a small effect on the fundamental impedance. Consequently, it will be necessary to iterate around the load-pull loop at least twice to get to that optimum point.

The first fundamental source pull for gain is shown in Figure 3.
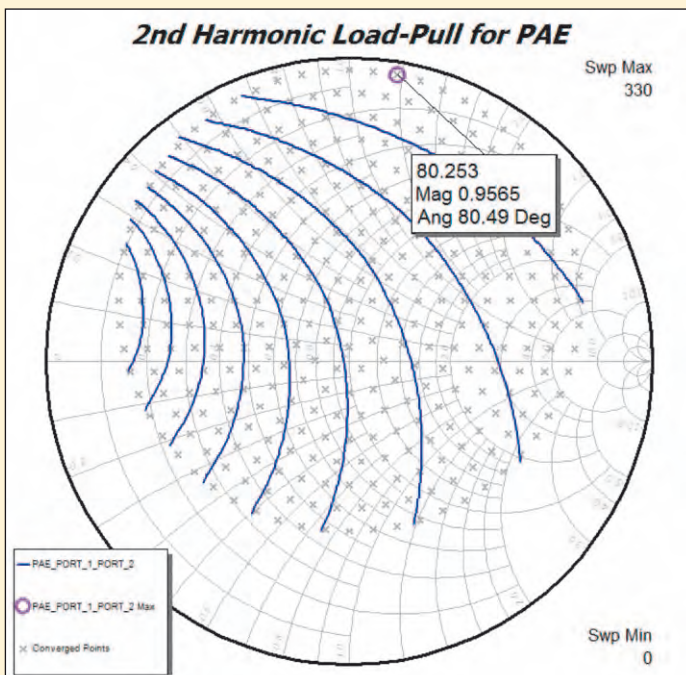

Figure 9: Both ports are loaded for optimal PAE, which improves to >80 percent when the second harmonic is properly terminated.
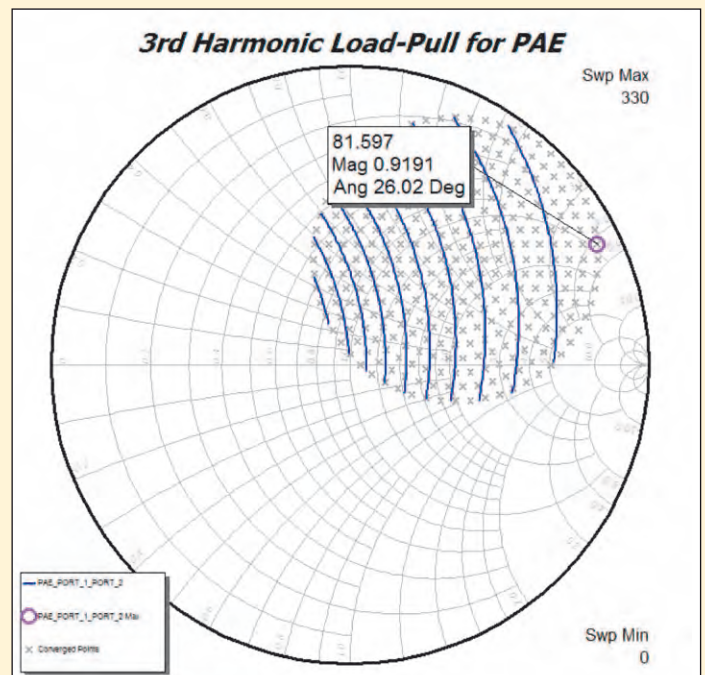

Figure 10: The third harmonic load-pull result has a smaller effect, providing one or two percentage points improvement in efficiency.
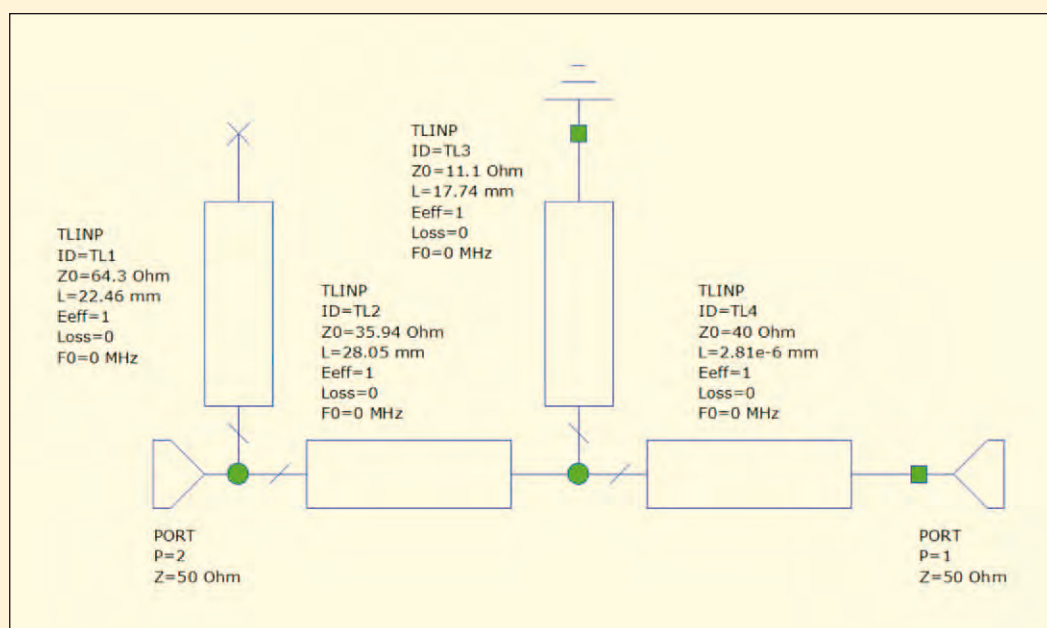
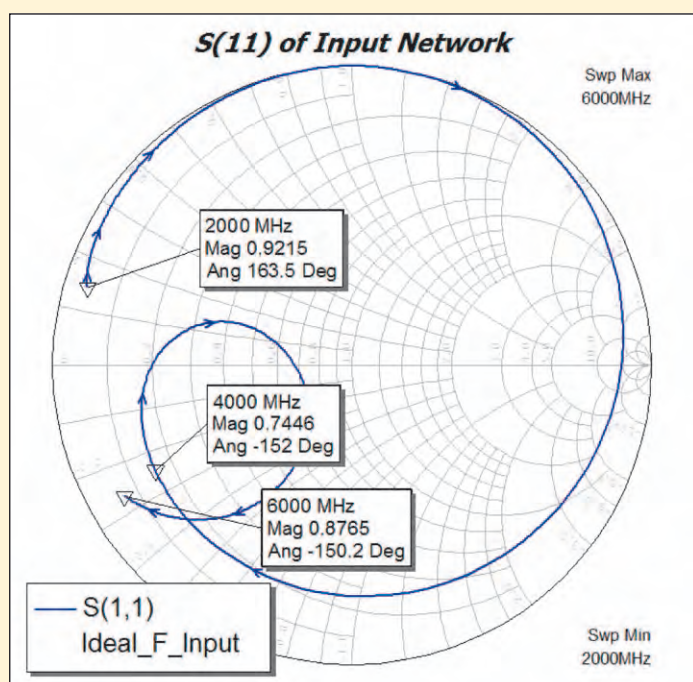*Figure 11: An ideal Class F input network.*

Figure 12: Terminations based on load-pull analysis.

The optimum impedance point is automatically calculated through all the converged points by the wizard. Remember, however, that the output of the device is loaded directly into 50 ohms, so although there is quite good power gain of 15.3 dB at the optimum point, the gain decreases (blue contours) away from that optimum point (magenta). Figure 4 shows the results for output power, which are actually quite close to those obtained for power gain, even though the output of the device is loaded into 50 ohms. To some extent, this is due to the fact that the intrinsic load line of the device is not that far from 50 ohms, as will be seen when fundamental load pull is performed.

Finally, Figure 5 shows the fundamental source pull for PAE. Again, the optimum point for PAE has an impedance that is very close to the maximum for both gain and power, which simplifies the matching task considerably. Note that even though the load is directly into 50 ohms, the PAE is already over 60 percent at this point.

The next step is load pull for maximum gain (Figure 6), with the source pull set at the impedance that was giving the best PAE. Now it can be seen that the optimum impedance for gain in this case on the load side of the device is not that far removed from 50 ohms - about a two-to-one voltage standing wave ratio (VSWR).

Figures 7 and 8 show the fundamental load-pull results for power and PAE. The result for power is similar to the impedance point for gain, with a small difference seen for the optimal PAE result. The PAE has improved from 60.5 percent with source pull alone to 72 percent at this point, with both ports matched for PAE at the fundamental only.

Using the load-pull wizard, there are several options for source and load-pull optimization at the second and third harmonics. Figure 9 shows the result with the fundamental source and load impedances set to previous values and, then allowing the wizard to find the optimum second harmonic load pull for maximum PAE. In this case, the PAE has improved to over 80 percent. Adding the third harmonic load pull (Figure 10) has a smaller effect, improving PAE by one or two percentage points.
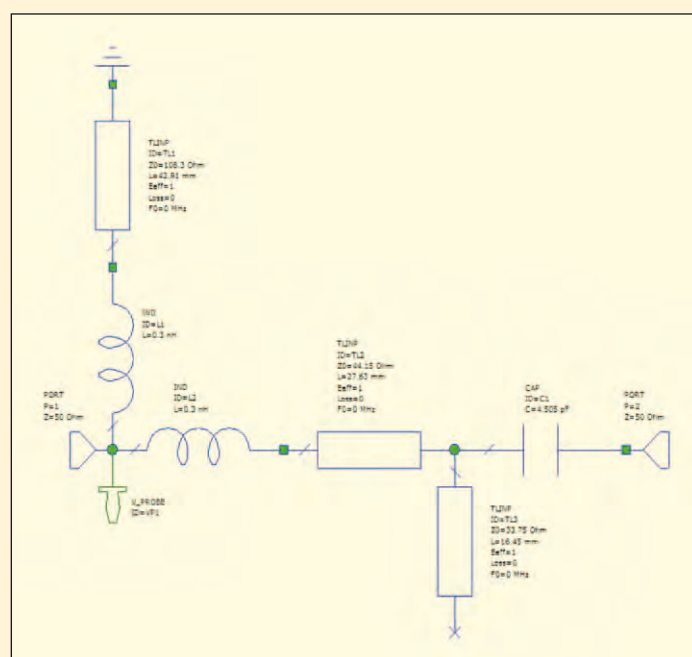

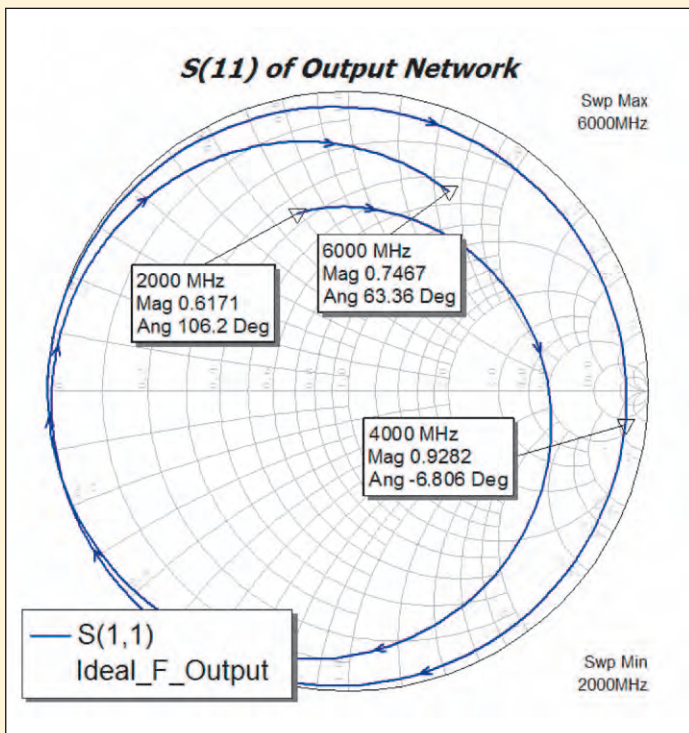*Figure 13: Harmonic loading: open at second and short at the third.*

Figure 14: Terminations based on load-pull analysis. The λ/4 shunt transmission line, also used for the drain bias, is high Z for odd harmonics, low Z for even harmonics.

Using the load-pull data

Now that the optimum fundamental, second, and third harmonic terminations have been achieved, the PA design can be implemented. This example is a relatively narrow-band design centered at 2 GHz, using the CGH40010F transistor. Matching networks will be synthesized that as closely as possible transform the 50 ohm input and output to the required device impedances over the entire frequency range. Of course, the practical networks that are produced will emulate the impedances that have been defined, but they won't exactly match them.
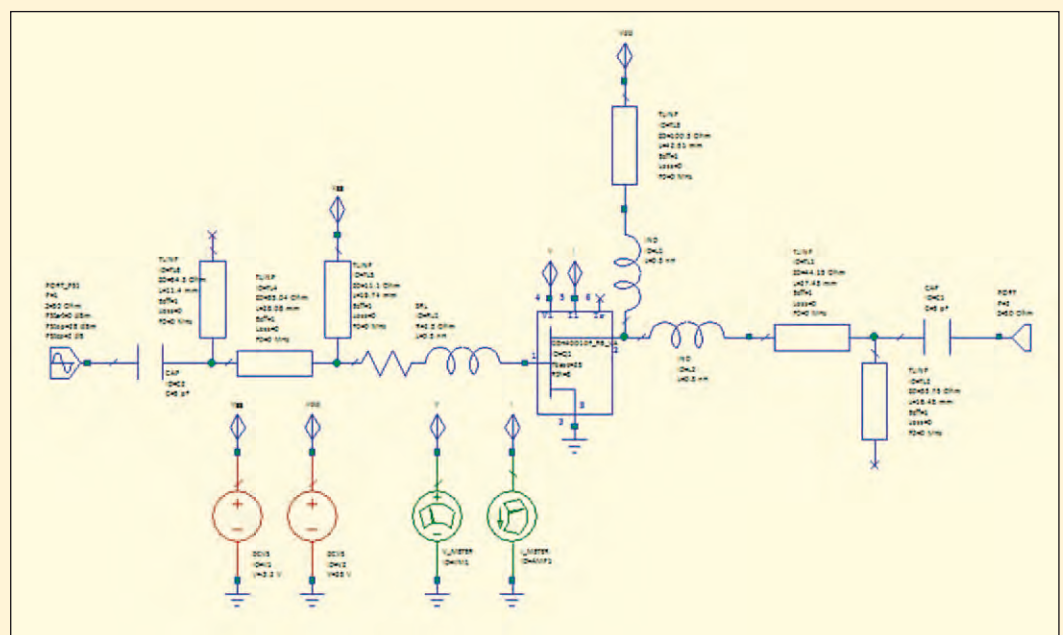
The ability to perform source pull and load pull for the device at the second and third harmonics can be used to meet other performance goals. For example, the same kind of optimization can be done to maximize power gain and output power for a particular PA design.

The ideal input network for a Class F PA is shown in Figure 11, which in this case consists of transmission lines, plus a short-circuited stub on one side and an open-circuited stub on the other. The impedance transformations and harmonic terminations of this network closely approximate the values determined by the previous series of source-pull optimizations.

The S11 of that input network is plotted in Figure 12, showing the result at 2, 4, and 6 GHz. If those impedance points are compared with the previous ones that the wizard was predicting, it would be found that they are not exactly the same. This is because physical implementation introduces some differences between the practical network and the ideal impedance points.

Figure 13 is the ideal Class F output. The quarter-wave line is also used to provide drain bias for the transistor. In addition, there is an open circuit stub with some transmission line transformation, so that it is an open at the second harmonic and a short at the third harmonic.

Looking into the input of the network from the location of the device drain, Figure 14 shows the fundamental, second, and third harmonic impedances presented by the network. Again, going back to the wizard, it can be seen that there are some differences between the practical transmission line-based network and the ideal impedances.

In Figure 15, the networks are placed at the input and output of the GaN HEMT device and a simulation of the complete amplifier is run.

Figure 16 is the simulated prediction for power gain, output power, and PAE. The results show that PAE reaches a maximum of 84 percent, which is slightly better than the result predicted by the load-pull wizard.

Figure 17 shows the drain voltage and current waveforms. Recall what was noted earlier: when source and load pull are done with the Microwave Office Load-Pull Wizard, users will get some degree of waveform engineering. If they tell the wizard that they want to have maximum PAE, the wizard's optimization algorithms will try to produce the voltage and current waveforms at the transistor that are not only the right shape, but also ideal and anti-phase.

The waveform plot shows an approximate square voltage waveform, or as close as we can get by engineering only a few harmonics. The half-sinusoid current waveform is a much better approximation. These waveforms are measured at the device junction, so we do not

Figure 15: The complete PA, with input and output networks, gate and drain bias, and the CGH40010F GaN HEMT.

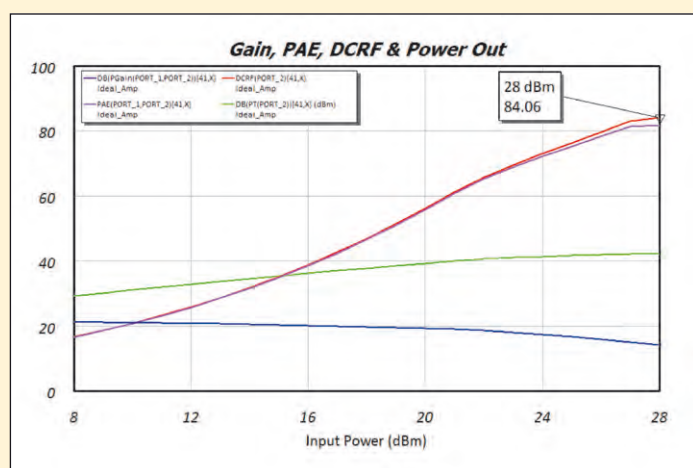*Figure 16: The simulated prediction for power gain, output power, and PAE.*

Figure 17: Voltage and current waveforms.

have to worry about the effects of parasitics between the device and the model pins. The new Cree GaN HEMT models have additional pins (see Fig 15) that allow us to measure directly at the junction to see the transistor waveforms [7].

Another feature of this design is in the harmonic content as seen at the output of the amplifier (Figure 18). This is not at the drain of the amplifier, but at the output. From this data, it can be seen that the harmonic terminations are doing their job well as there is very little harmonic content coming through the output of the amplifier.

Output power varies by 1 or 2 dBm across 200 MHz, so it is an inherently narrow-band design, as are most Class F PAs.

Figure 19 shows the PAE versus frequency and it can be seen that it is in the range of 80+ percent over about 150 MHz but drops off quickly on either side at 1.9 and 2.05 GHz.

Conclusion

In conclusion, switching modes of operation for PAs such as Class F and Inverse Class F are becoming more and more popular as designers focus on improving PAE.

This is true for a range of applications from radar to wireless telecom. The Microwave Office Load-Pull Wizard and its ability to inspect transistor voltage and current waveforms helps designers gain confidence in their high performance designs and the process of waveform-engineered PA design.
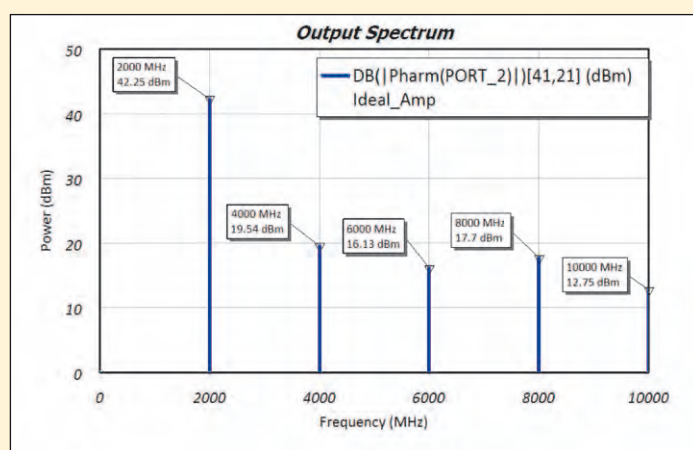
Bibliography

1. P. Colantonio, F. Giannini, E. Limiti, High Effi ciency RF and Microwave Solid State Power Amplifiers, John Wiley & Sons, Ltd, 2009.

2. A. Grebennikov and N.O. Sokal, "Switchmode RF Power Amplifiers", Newnes, 2007

3. V.A. Borisov and V.V. Voronovich, "Analysis of Switched-Mode Transistor Amplifier with Parallel Forming Transmission Line", Radiotekhnika Elektronika, vol. 31, pp. 1590-1597, August 1986.

4. M.K.Kazimierczuk, "A new concept of Class F Tuned Power Amplifier", Proc. 27th Midwest Circuits and Systems Symp., pp. 2007-2012, November 1997.

5. T. He, "Design of Radio Frequency Power Amplifiers for High Effi ciency and High Linearity", A Thesis Presented to the Faculty of California State University, Chico, 2009. http://csuchico-dspace.calstate.edu/xmlui/bitstream/handle/10211.4/168/ 10%20 19%202009%20Tien%20He.pdf?sequence=1

6. A. Grebennikov, "Load Network Design Technique for Class F and Inverse Class F PAs", High Frequency Electronics, pp. 58-76, May 2011

7. R. Pengelly, "The new Cree 6 port intrinsic GaN HEMT large signal models – aids waveform engineering of PAs and deeper understanding of PA operation", Cree RF Products, October 2013.

Figure 18: At the output, there is >23 dB worst-case harmonic rejection, confirming that terminations are working properly.

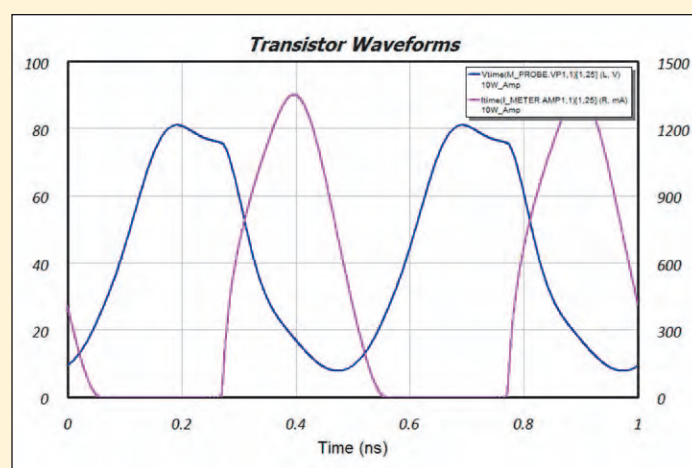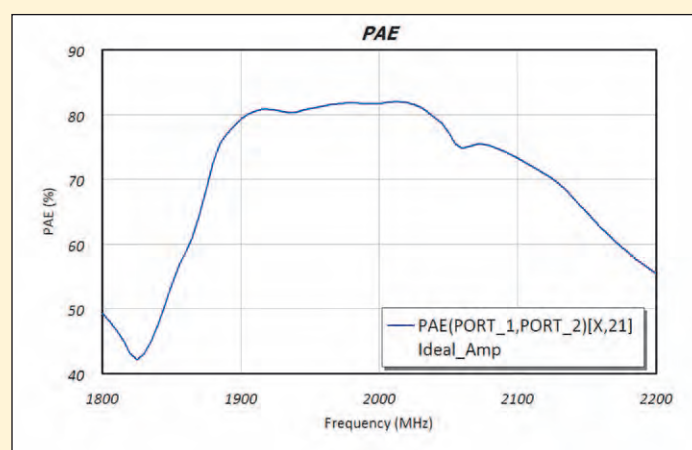*Figure 19: PAE versus frequency. PAE remains relatively constant over 150 MHz, but drops off quickly below 1.9 and above 2.05 GHz*